

An Optical Fiber Based DAQ System for Silicon Microstrips Detectors

C. Civinini¹, R. D'Alessandro¹, M. Meschini¹

¹University of Florence and INFN-Firenze, Lgo. E. Fermi, 2, I-50125 Florence, ITALY

Abstract

We describe a completely optically decoupled DAQ system, using a single optical fiber for feeding fast trigger and control signals to the front end electronics.

I. INTRODUCTION

We have built a new DAQ system that has been designed keeping in mind its eventual use in test beam and laboratory environment. The system uses extensive decoupling schemes allowing a fully floating connection to the detector. This feature has many advantages especially in the readout of the latest double-sided silicon microstrips detectors being developed for the high energy physics experiments. Furthermore, scalability and evolving requirements dictated by the front-end chips used for the detectors are easily implemented by the use of reprogrammable arrays in the logic boards.

The system is based on VME and uses standard VME CPUs for data formatting and for storage on disk [1]. Signals from the silicon front-end amplifiers are converted and immediately sent to the FIFO buffers located on a VME board via an optical Foxi link. Data transmission to the VME CPU and data storage are concurrent with the digitization thus eliminating data transmission overhead.

II. SEQUENCER AND INTERFACE BOARD

A custom designed sequencer based on the MAX9000 serie chips by ALTERA corp. provides the fast trigger (upon assertion of the appropriate input from an external triggering device) and the clock sequences needed by the front end silicon detector chips (i.e. PREMUX). The system is versatile enough as to be used also with other chips like the VA series. Furthermore the sequencer has a serial RS232 input through which a number of variable parameters of the sequence can be set, thus allowing users a wide choice of computer platforms for running their DAQ.

The sequencer is connected to the front-end hybrids with an optical fiber through an Interface board. Care has been taken to minimize delays for the trigger signal, which in the case of the PREMUX chips must arrive within 50 ns of the particle crossing in the microstrip detector. The delay between trigger input to the sequencer board and hold signal generation on the Interface board, using a 2 meter long fibre, is of the order of 30 ns.

The Interface boards receives and decodes the optical signals producing all the commands to drive the Premux. This board uses a MAX 7000 programmable array to decode the sequencer signals; it also provides for analog signal buffering to the ADC converters. Calibration signals with various amplitudes and timings with respect to the hold signal are also generated on board, thus allowing a full check-out of the hybrid

without the need of any external components and connections.

The parameters which can be set by the user through the serial port to the sequencer and which are then decoded and properly generated by the Interface board are:

1. Number of strips to read (1 to 1024).
2. Frequency of strip multiplexing (from 400 ns to 12 us per strip)
3. ADC sampling delay (from 25ns to 10 us depending on multiplexing frequency)
4. Calibration mode or beam mode
5. Calibration level (from 0.75 MIP to 5 MIP (Minimum Ionizing Particle equivalent charge))
6. Delay between calibration signal and hold signal (from 14 ns to 90 ns)

The last item allows for a full premux pulse shape reconstruction needed for the optimal choice of hold signal delay.

One important feature of the Interface board, is that there are no clock signals present on the board. The board thus sits quietly without disturbing in anyway the Premux chips. On arrival of the trigger pulse the hold signal is generated and only when the analog information is safely stored in the Premux multiplexer the readout sequence begins.

III. ANALOG TO DIGITAL CONVERTER AND VME SYSTEM

The analog signal coming from the detector is amplified on the interface board then sent to the Flash ADC board through a twisted pair shielded cable. The ADC boards used have also been designed by us and are based on a low-power 20 MegaSample Flash ADC. The system is described in [1], together with the VME setup. The digital outputs are sent to the rest of the readout system through optical links (Foxi); is it also possible to use, through a suitable simple adapter, a Taxi link. A VME board (FOXI board) receives the data and provides fast memory buffering while the CPU transfers the data to disk. Each board can read up to 12 electronic chains, with 32Kbyte buffering for each chain. In theory one could daisy chain up to 32 hybrids (1024 strips each) per electronic chain and so read out 384 modules per board, or else use the fast buffering for high speed readout of 12 modules.

IV. CONCLUSIONS

Using this DAQ system, we have electrically decoupled the silicon modules from each other. This, together with the use

of floating power supplies, allows us to refer each electronic readout chain (silicon, hybrid, interface boards and ADC) to the bias voltage used for each individual silicon module.

The freedom given by the system is a necessary condition, for silicon microstrip detector studies in laboratory and on test beams.

V. REFERENCES

- [1] C. Civinini et al., to be published in IEEE Transaction on Nuclear Science, paper number NSS/MIC97-98.