

## Final FED Status & Requirements

- Last Meeting we looked at FED Interfaces and Requirements  
*“User Requirements Document for the Final FED”*

Public Draft available soon... Ian Tomalin et al

- Final FED Production Strategy

**FF1** - prototype for 2002 Q3

Interfaces/Functions needed for rod & petal tests

+ additional functions: eg. Cluster Finding, S-Link...

**FF2** - pre-production for 2003 Q4?

The Final design.

Hopefully only minor changes from FF1.

**FF3** - ≈x500 production for 2004 Q1?

Fixes any bugs found in FF2.

FED-PMC (FF0)-

Design fixed (only very minor firmware mods permitted)

No further production runs envisaged.

Still needs support for lab tests, Test Beams etc.

- Development Status **FF1** Design

Front-End FPGAs -

Basic Cluster Finding design done, simulated, synthesised

Next : Raw data, Frame Sync, Phase adjustment, Controls..

Back-End FPGA -

I/O being finalized,

including Front-End to Back-End FPGA links

## FED Crate Layout

### FED Modularity

Total number of FEDs  $\approx$  **430**

$\approx$  **18** FEDs/crate  $\Rightarrow$  24 crates

3 crates/rack  $\Rightarrow$  **8** racks

1 “Crate Controller” (PC)/rack  $\Rightarrow$  **8** Crate Controllers

**240** DAQ S-Links (NB. varies from **6** to **18** / crate)

But...

- How is Tracker Partitioned for TTC?

- 4** partitions (naïve)?

- Barrel x 2 halves

- End-Cap x 2

- 4 (6)** partitions?

- Inner Barrel x (2 halves)

- Outer Barrel x (2 halves)

- End-Cap x 2

Implications:

- Can't mix inner/outer barrel layers on S-Link

- $\Rightarrow \approx$  **270** DAQ S-Links

- Can we mix FEDs from different partitions in same crate?  
and with same Crate Controller?

## DAQ Interfaces Revisited

### DAQ-Links

S-LINK 64 is specification of “FIFO like” Interface at pin level  
Physical implementation or protocol details are User defined

Assumption is Push protocol with back pressure control?

Likely Clock rate, max 100MHz?

CMC plug on with Optical Link (connection on Front Panel)

### Trigger Control System-Links **Outwards** to Fast Monitor Unit

- *Ready*

- *Busy*

- *Warning Overflow* => send Empty events

+ *Out of Sync* (L1Reset), *Error* (HReset), *Cal* (request Calibrn)??  
(via CC slow signals)

Only 1 Group/TTC Partition at input to TCS (LVDS) (Our  
responsibility to transmit/merge signals)

### TTC Inwards

Can we (ab)use Trigger Type Chan B broadcast for Pipeline # ?

Do we need to count orbits? Time stamp from GLT?

FED L1Reset via ChanB (cf FEC ‘101’) resets pipelines, L1A,  
BX. How long do we have?

HReset via ChanB. What to do & How long do we have?

Periodic Local APV resets when **no triggers** in pipelines?  
(SEU) a la Pixel... private orbits used for APV resets?

Doesn't reset FED L1A,BX but Header Sync logic?

