

# PC based test-bench at CERN



Simple basic PC + VME system ----- Operational in bldg.14  
S. Marchioro's lab

a PC running Linux with min 3 PCI slots housing

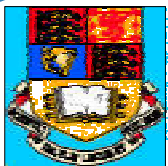
- \* PMC FEC (passive carrier required)
- \* PMC FED " " "
- \* Bit-3 interface card with VME

- \* 1 CCU card
- \* 1 TRI card
- \* 1 Si module
- \* 4 APV6

VME crate with:

- \* SBS 617 interface with PC
- \* TTCvi + TTCvx
- \* Sequencer

- \* Digital Optical fibers from TTCvi to FEC
- \* Digital Optical link for Control Ring



# Software

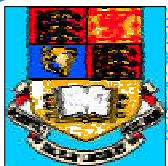


## Low level software hidden to the user

- \* Linux drivers ( C ) for FEC, FED, Bit3
- \* 2 servers for FEC and FED ( C++ ): interface with the hardware by opening the corresponding device file, read and write data

In collaboration with  
L. Mirabito  
M. Ageron

- \* FEC and FED clients to change parameter setting, data analysis, monitoring ....  
Qt based client tasks



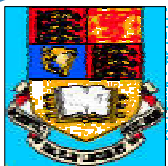
## Move to APV25



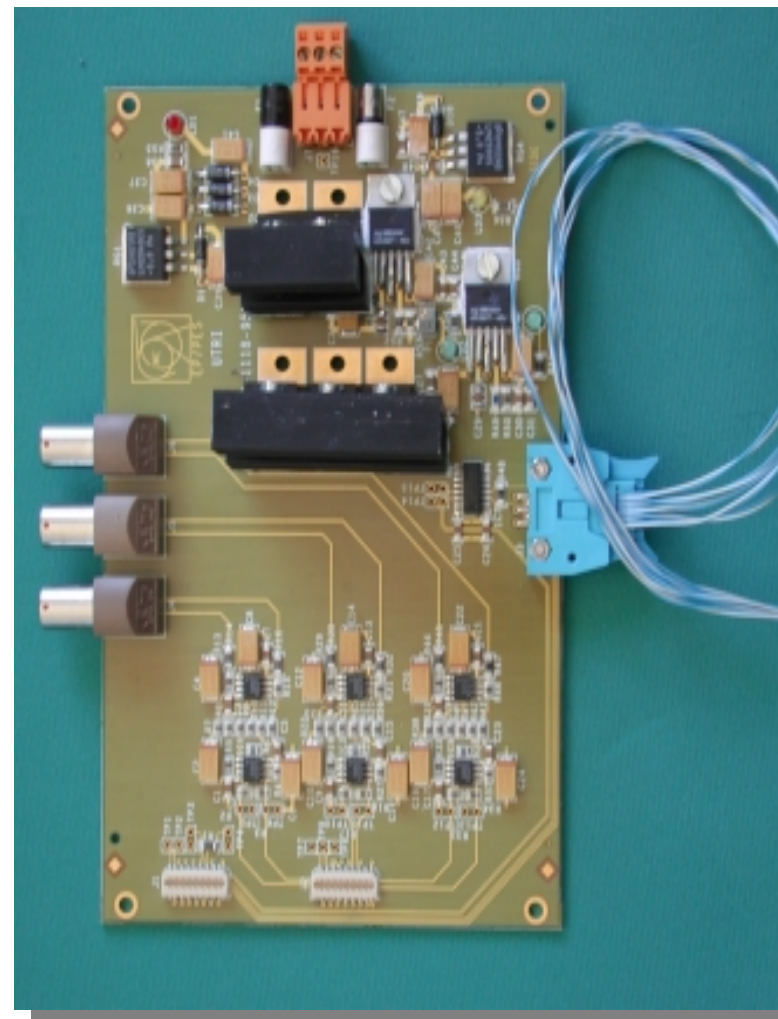
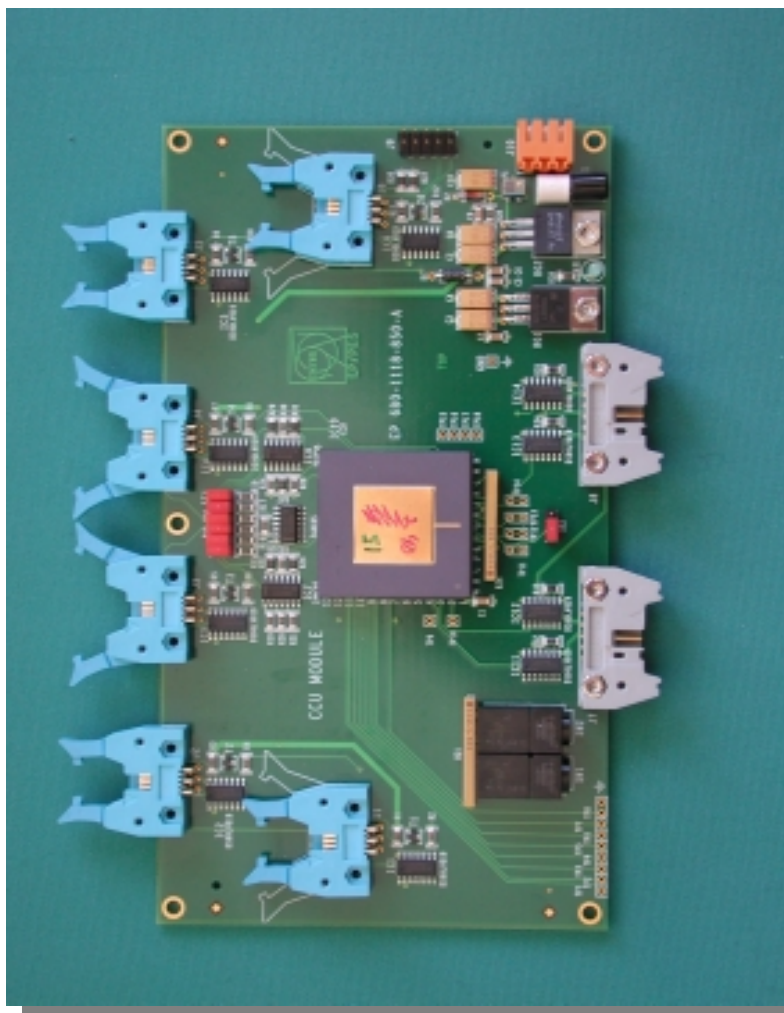
- 1) APV25 + new hybrid,
  - 2) New CCU card ( different I2C levels for APV25)
  - 3) UTRI card
- 2), 3) already installed in the system and working

### Needed:

- \* Update the APV6 dependent part of Laurent's Control code to work with APV25  
Done .... To be tested.
- \* Drive I2C of the new PLL-MUX chip  
Code in preparation (always using the Lyon building blocks ..)
- \* Update the version of the FED firmware to get data from APV25  
( a problem with the header recognition discovered and fixed )  
The version to be used is fpga\_v2r40p.rbt (see RAL website)



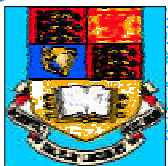
# New CCU Module & UTRI



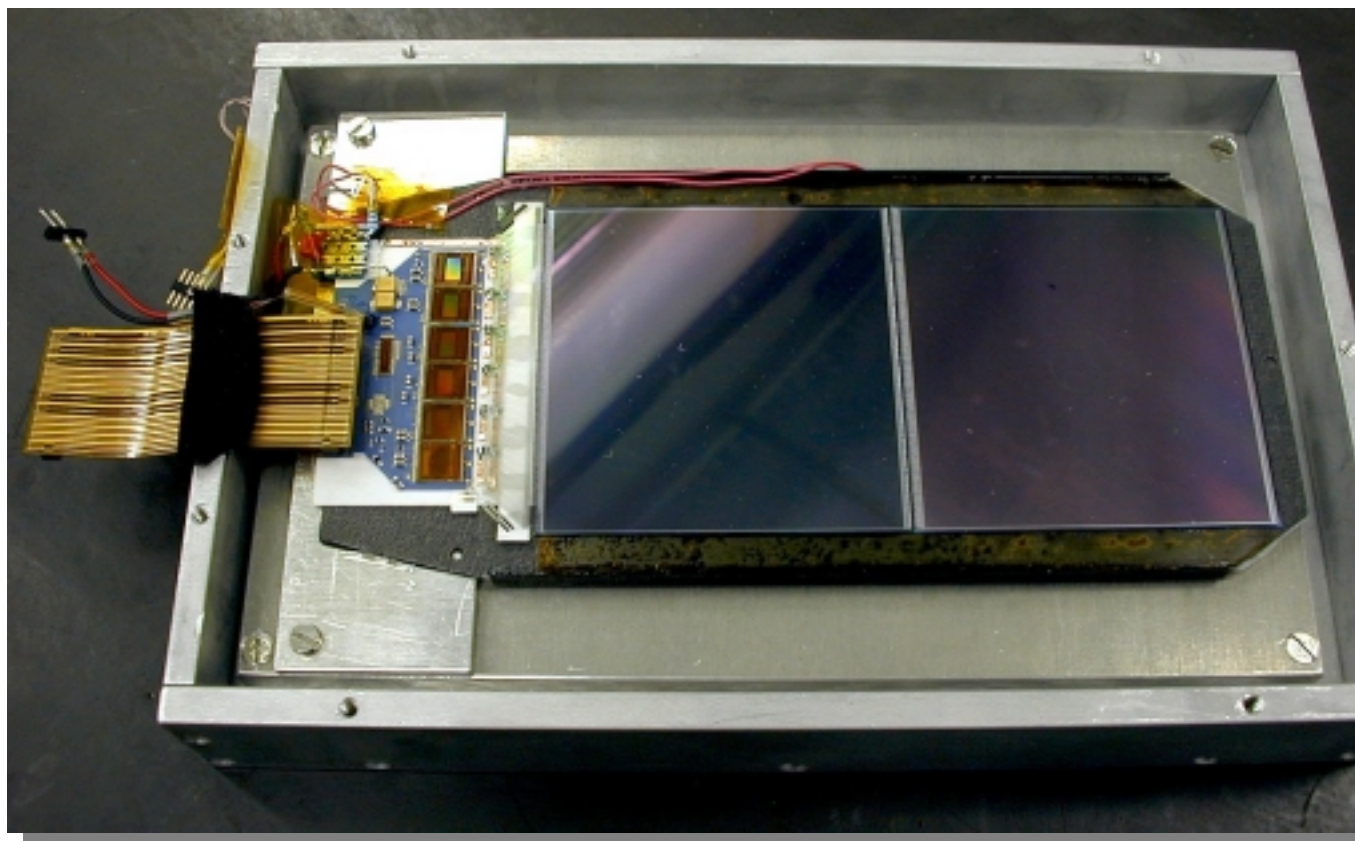
Module Test Meeting 05/03/01

N. Marinelli

Imperial College-London



## CERN Si module + new hybrid



**A. Honma: module fully assembled. No bonding between APV and module yet to allow for testing the bare hybrid**