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Procedures For CMS Silicon Tracker Module Testing Using ARC System

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Abstract

In this note we describe the testing procedures and quality selection criteria, as agreed in the CMS Module Test Working Group in Autumn 2003, to be applied to the silicon microstrip detector modules of the CMS tracker. The procedures are optimized for fault finding and defect identification, based on a minimal set of compulsory tests to be performed with ARC test setups used in CMS testing facilities. We describe also the use of a macro capable of analyzing standard ARCS ROOT output files.

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1 Introduction

A module testing task force has been set up in order to study the optimization of the module qualification procedures during the production of the CMS silicon tracker modules. This task force met in Torino in July 2003. The results of its work were presented in different meetings and were endorsed in Autumn 2003. The goals of the meeting were the following:

- Using modules of all types available, determine the necessary characteristics for a module test stand.
- Define the minimum set of tests necessary to identify bad channels efficiently without a large mis-tag rate
- Determine the best cuts for these tests using the cumulative distributions of tested modules available
- Develop an automated method of fault type identification and provide an analysis macro to testing community for the validation of the module production
- Identify the necessary changes to the ARC [1] and LT [2] software in order to incorporate the analysis routine into the software itself and generate the xml output for the central database

The task force focused on module tests using the ARC hardware and software, as it is currently the primary test stand for fault finding in the community. The overall testing strategy was optimized to find all defects, at the expense of a slightly higher mis-tag rate (marking good channels as bad). The testing procedures given are intended for module production. Using the procedure outlined, results from different testing centers should be easily combined, which will allow for the quick feedback necessary for the final optimization of the assembly/testing procedures.

Procedures for module testing using the CMS-like test setup and for hybrid+pitch adapter (PA) testing will be forth coming.

2 Required Tests

All groups should use the following three tests to flag bad channels:

- Noise Measurements (in all four APV modes(1)): identify pinholes, PA-sensor and sensor-sensor opens, and shorts and is rather insensitive to local noise sources when properly grounded and held in proper fixturing. (See section 3 for details.)
- Pulse Shape Test (in all four modes):
  - Peak Time: identifies pinholes, PA-sensor and sensor-sensor opens and is insensitive to grounding scheme and local noise sources.
  - Pulse Height: identifies shorts and pinholes
- Pinhole Test: identifies pinholes and noisy channels and is insensitive to grounding scheme and local noise sources.

The failures in these three tests can be correlated to definitely identify the fault type of the channel (see section 6 for details). To do this, various failure levels have to be defined and assigned in each test. By requiring confirmation of failures in multiple tests, we often avoid incorrect bad channel flagging due to statistical fluctuation in one test.

A set of macros which analyze the ROOT output of the ARC software starting from version 6.0 has been developed and can currently identify both open types, pinholes, noisy channels, and shorts. The analysis algorithms are described more thoroughly in section 8. Macros are available at the module testing working group web page [3]; the macro's channel flagging algorithm has been integrated into the current version of the ARC software. As more modules are tested, the analysis code and requirements will be updated.

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(1) Peak Inverter Off, Peak Inverter On, Deconvolution Inverter On and Deconvolution Inverter Off

3 Test setup requirements and suggestions

Two requirements have been shown to be necessary for uniform testing: a low common mode noise (< 0.4 ADC counts for one sensor modules, < 0.5 ADC counts for two sensor modules, in Peak Inverter Off) and a low relative humidity ($< 30\%$) environment. The low common mode noise requirements were shown to be necessary for the identification of opens; with a common mode noise higher than these requirements it has been shown that opens can have the same noise performances as regular channels [4]. The $< 30\%$ RH specification was provided by the sensor group; any test performed above 30% RH can have surface current effects which can cause extremely large noise and/or currents.

A careful investigation of grounding, shielding and cabling is needed at each testing center, as the common mode noise performance of the test stand depends on the details of the power supplies used, the local environment, and the module plate and holder. Some general guidelines are given below that have been shown to improve the noise performance at different testing centers.

A continuous, thick (> 2 mm) shield around the test stand has been shown to significantly improve the noise performance of test stand at many test centers. It has also been shown that isolation of the module holder from the shield improves the noise performance.

Thick, short ground connections between the hybrid-to-utri adapter card and either the shield (Tracker Outer Barrel, TOB) or the support plate (Tracker Inner Barrel, TIB) has also been shown to minimize the common mode noise. The ground connections should be made as close as possible to the hybrid. Floating LV/HV power supplies also can decrease the common mode noise, but have not been shown to be absolutely necessary. Isolation of metal (cold ledges, LED systems) near the module's sensors with a thin piece of kapton tape has also reduced the common mode noise in TIB modules. Finally, the addition of more filtering capacitors on the HV bias lines has also improved the noise performance of TIB modules expecially on the sensor edge channels. References [4] and [5] give a more detailed description and picture these suggested improvements.

4 Required Testing Procedure

This section describes the required tests for module qualification/fault finding using the ARC stand and ARC version 6.0 or later software. This testing procedure attempts to be a natural modification of Ref. [6]. The initialization settings used in the test should match those in Ref. [6]. The variables used in this note are the same as in Ref. [6]. First an overall list of the required tests is given, followed by a complete description of each testing step.

The following tests are required:

- All Fast Tests (Pedestal and Calibration Pulse Tests are not used for flagging bad channels)
- IV Test
- Pedestal & Noise Test (in all four modes)
- Pulse Shape Test (in all four modes)
- Pinhole (Continuous LED) Test in Peak Inverter Off (only mode available)
- Pulsed LED Test in Peak Inverter On (only mode available)
- Pipeline in Peak Inverter On

The IV Test should be performed between 0 V and 450 V bias. All other tests should be performed at 400 V.

4.1 Fast Test

The automated fast tests check the basic functionality of all the ICs on the hybrid (APV, DCU, MUX, and PLL). Any failure would indicate a gross problem for an entire chip. In order to get the correct ARC output, this test should be performed at 400 V.

4.2 IV Test

The module's IV first must be measured by bonding only to the bias ring and to the backplane (when applicable), until it has been shown that assembly/bonding is not deteriorating the IV performance of the modules. After this measurement, the sensor strips should be bonded and the IV re-measured. The sensor bias voltage is to be ramped up to 450 V at a maximum rate of 10 V/s; the bias current values should be recorded every 10 V. The relative humidity must be less than 30% during this and all other measurements.

The IV measurement needs to be temperature compensated to compare the measurement at the sensor probing center (T_0) and the module measurement (T). The formula for the temperature compensation is:

$$I(T) = I(T_0) \cdot (T/T_0)^2 \cdot e^{-7100 \cdot (1/T - 1/T_0)} \tag{1}$$

where T and T_0 are measured in Kelvin. The measurement of the IV of the sensor(s) in the sensors database needs to be retrieved in order to compare to the module measurement. The ARC software allows for the input of the sensors database and module IV measurements from a text file into the ARCS IV page to allow for easier module grading and xml generation.

4.3 Pedestal & Noise Test

The pedestal & noise test must be performed in all modes at 400 V. 2000 events must be taken in each mode. For a more accurate common mode noise evaluation, its calculation should use the mean of groups of 32 channels. To be considered a good test, the common mode noise in Peak Inverter Off must be less than 0.4 ADC counts (0.5 ADC counts) for one (two) sensor modules. The ARCS displays the RMS of common mode distribution per chip for easy verification.

4.4 Pulse Shape Test

The pulse shape test also must be performed in all four modes at 400 V. During the pulse shape test, the amplitude and peaking time of the calibration pulse is measured. A calibration signal equivalent to 2 MIPs should be used. A minimum latency of 14 and a maximum latency of 18 is sufficient to measure the peak time and the pulse height accurately. At each step, 10 events should be taken.

4.5 Pinhole Test (Continuous LED Test)

The pinhole test also should be performed at 400 V. Calibration at fixed latency are taken with a constant illumination, stepping the amount of illumination during the test. The leakage current induced by the illumination saturates/unsaturates pinholed channels. This is detected by a change in calibration pulse amplitude as a function of illumination. The LED setting should be set at the maximum value (3) which yields a bias current of 300 $\div$ 400 μA. 5 events should be taken at each illumination step.

4.6 (Pulsed) LED Test

This test is performed in one APV mode (Peak Inverter On) at 400 V bias and it has the possibility of being a powerful tool for open finding. For the pulsed LED test to work properly, the LED system needs to be mounted 3 mm $\div$ 10 mm from the sensor surface. The data are taken for future reference.

4.7 Pipeline Test

The APV pipeline test has the potential to find bad pipeline capacitors which could be used, for example, to determine why a certain channel is noisy. A total of 100 events per cell should be taken in Peak Inverter On mode.

4.8 Additional optional tests

Two additional tests may be useful in finding faulty channels, but as of now are not yet fully implemented. The first test is backplane pulsing, which is primarily designed to find opens, but has the potential to find pinholes as well. The ARC software with the new ARC FE includes the possibility of performing this test. The forward biasing test has the potential to find pinholes that the standard pinhole tests may miss. In addition, this test could be performed during module and substructure testing, where LED test is not available. More information on this test is available in [7] and in [8].

5 Bad Channel Definitions

Until now, two sets of bad channel cuts have been defined for 512 strips modules: one for one sensor modules and the other for two sensor modules. When the number of modules of a given type becomes significant, the cuts for a given module type may have to be tuned, as the load capacitance changes with strip pitch and length. A channel failing any of the cuts in any mode is marked bad, except for the first or last strips of a module that only fails the noise requirements. At present we are using the logical OR of all possible failures because we want to be conservative and avoid missing any really bad channel. This can eventually lead to flag as bad a few good channels. This strategy can be revised after significant statistics have been accumulated.

Multiple bad cuts levels are used in the noise and peak time test to try to identify fault type and location. The next subsections give the current cut values and the letter codes used in the analysis macro to indicate a given failure.

5.1 Noise Test Requirements

The common mode subtracted noise (N_i) is used for bad channel flagging. The cut values for both inverter modes are the same. The current cut values are:

Cut Value Peak (1 sensor)	Cut Value Deconvolution (1 sensor)	Fault ID	Summary Letter
$N_i < 0.65$ ADC	$N_i < 1.0$ ADC	Pinhole	P
$0.65 < N_i < 0.95$ ADC	$1.0 < N_i < 1.3$ ADC	One Sensor Open	O
$N_i > 1.45$ ADC	$N_i > 2.0$ ADC	Noisy	N

Cut Value Peak (2 sensor)	Cut Value Deconvolution (2 sensor)	Fault ID	Summary Letter
$N_i < 0.6$ ADC	$N_i < 0.95$ ADC	Pinhole	P
$0.6 < N_i < 1.0$ ADC	$0.95 < N_i < 1.4$ ADC	One Sensor Open	O
$1.0 < N_i < 1.3$ ADC	$1.4 < N_i < 1.7$ ADC	Two Sensor Open	T
$N_i > 2.0$ ADC	$N_i > 2.4$ ADC	Noisy	N

5.2 Pulse Height Requirements

The chip normalized pulse height ($CPPA_i$) is the channel pulse height divided by the chip's average pulse height. The current cut values are:

Cut Value Peak (1 sensor)	Cut Value Deconvolution (1 sensor)	Fault ID	Summary Letter
$CPPA_i < 0.85$	$CPPA_i < 0.8$	Low Pulse Height	L
$CPPA_i > 1.15$	$CPPA_i > 1.2$	High Pulse Height	H

Cut Value Peak (2 sensor)	Cut Value Deconvolution (2 sensor)	Fault ID	Summary Letter
$CPPA_i < 0.85$	$CPPA_i < 0.8$	Low Pulse Height	L
$CPPA_i > 1.15$	$CPPA_i > 1.2$	High Pulse Height	H

5.3 Peak Time Requirements

The average subtracted peak time ($CPPT_i$) is the chip's average peak time subtracted from the channel's peak time. The current cuts are:

Cut Value Peak (1 sensor)	Cut Value Dec. (1 sensor)	Fault ID	Summary Letter
$CPPT_i < -30$ ns	$CPPT_i < -30$ ns	Pinhole	P
$-30 \text{ ns} < \mathrm{CPPT_i} < -5$ ns	$-30 \text{ ns} < \mathrm{CPPT_i} < -3$ ns	One Sensor Open	O
$CPPT_i > 5$ ns	$CPPT_i > 5$ ns	Noisy	N

Cut Value Peak (2 sensor)	Cut Value Dec. (2 sensor)	Fault ID	Summary Letter
$CPPT_i < -30$ ns	$CPPT_i < -30$ ns	Pinhole	P
-30 ns $< \mathrm{CPPT_i} < -8$ ns	-30 ns $< \mathrm{CPPT_i} < -4$ ns	One Sensor Open	O
-8 ns $< \mathrm{CPPT_i} < -4$ ns	-4 ns $< \mathrm{CPPT_i} < -2$ ns	Two Sensor Open	T
$CPPT_i > 10$ ns	$CPPT_i > 10$ ns	Noisy	N

5.4 Pinhole Test Requirements

The maximum pulse height difference for a given channel in the light intensity scan (PH_i) is used to find pinholes. $PH_i > 40$ ADC counts is used to flag pinholes (P).

5.5 Pedestal Test

The pedestal test is not used in bad channel flagging but has been included in the analysis macro for historical reasons. A $\pm 20\%$ requirement around the chip's mean pedestal will flag a channel in this test. The channel is marked as K if the pedestal is below the pedestal requirement and J if the pedestal is above the pedestal requirement in the test summary files. It can happen that the pedestal baseline is too low for a correct noise calculation. In this case the operator should act on the VPSP register of the APV [9] to raise this baseline.

6 Fault Test Definitions

Bad channel flags for a given chip mode are combined to determine failure type. The fault analysis is sequential, with the last identification superseding previous ones. These bad channel flags and fault finding algorithms are directly implemented in the ARC software.

The fault flagging algorithm gives the confidence level for the identification. Faults with multiple consistent bad channel flags are given stronger confidence levels that ones with only one bad channel flag. The current fault finding codes used are:

- OSO+: one sensor unbonded (confirmed by both noise and peak time tests)
- OSO-: likely one sensor unbonded (only either in noise or peak time test)
- TSO+: two sensor unbonded (confirmed by both noise and peak time test)
- TSO-: likely two sensor unbonded (only either in noise or peak time test)
- PHL+: pinhole (confirmed by all tests)
- PHL-: likely pinhole (saturated channel)
- MSO-: possible mid-sensor open (fast peak time with high noise)
- NOIS: high noise channel
- SHT+: short (low pulse shapes and at least one channel non-normal noise)
- SHT-: likely short (only low pulse shapes)
- OPN?: likely open (conflicting location results in noise and peak time tests)
- ????: unidentified problem (conflicting test results)

The exact fault finding algorithm is given in appendix A.

7 Module Grading

Module grading as of now is fairly simple. A module is Grade A if the module has less than 1% bad channels. A module is Grade B if the module has between 1% and 2% bad channels. In both cases the module's IV test has to pass selection. Any module with more the 2% bad channels is Grade C.

7.1 IV Test

A module is graded C also if $I(450\,V) > 10\mu A$ per sensor. Moreover, a module is graded AF (BF) if it is a grade A (B) module and if the $I(450\,V) > 5 * I(450\,)_{DB}$, where $I(450\,)_{DB}$ is the bias current at 450 V from sensors probing database.

8 Analysis Macro

A root macro has been written that implements the above testing procedures (except for module grading) [3]; the testing procedures have since been integrated into the ARC software. The macro takes the ARCS ROOT file and a cut configuration file as inputs, and outputs test summary files, bad channel lists and postscript files. The macro assumes that all the test results are in the same root record and that all the required tests are performed; if a test is missing for the used record, the analysis macro is likely to misdiagnose problems.

In the cut input file, the directory and name of the input root file is indicated. The directory for the output file is chosen, as the record number used in the analysis. The directory for the output file must be created prior to running the macro.

The macro can be run on the UNIX command line using: root -b -l -q 'arcs_macro_6_x.cc("cut file","CTA",0)' where: "cut file" is the cut file to be used, CTA is a name to be added to the output ASCII and postscript files. For data files taken with the ARC 6.0 version, the arcs_macro_6_0.cc should be used. With all later version of the ARC software use the arcs_macro_6_1.cc.

8.1 Output File Descriptions

The macro has three output file types. Four summary files give the tests results for the four test modes, respectively, in a simple ASCII format which visualizes the correlations in the test results. See figure 1 for an example of the output. The bad channel list is also an ASCII file. It lists the fault type assigned to all the channels that have failed a test in at least one mode (see figure 2 for an example). The file allows the user to see if any unexpected bad channels have been found in a quick way, and if the fault is found in all modes. Finally, plots of all the cut variables in all four modes are shown in one page. Dotted horizontal lines indicates the values given in the cut files, and the red vertical lines show which channels failed the selection requirements. See figures 3 to 6 for examples of these plots.

9 Database

All the test result will be stored in a central database according to the tables described in Ref. [10]. All ARCS output files must be stored locally in each testing center for future reference.

References

[1] APV Readout Controller http://www.physik.rwth-aachen.de/group/IIIphys/CMS/tracker/en/index.html

[2] Longterm CMS Si Module Test http://hep.uia.ac.be/cms/testing/

[3] See "Tony's macros for ARCS 6.1 and later" on http://hep.fi.infn.it/CMS/marchett/production

[4] Study of grounding/environmental effects on testing http://hep.ucsb.edu/cms/xcalibration.ps

[5] Module Test Progress and Report on Torino Workshop http://hep.fi.infn.it/CMS/moduletest/tkwjul03/m-modif.pdf

[6] L. Demaria, M. Meschini, F. Hartman, G. Dirkes, *Procedures for Module Test (Draft 2)* http://hep.fi.infn.it/CMS/moduletest/procedures_2002/Test-procedures-draft2.pdf

[7] Module Test and Xcalibration with the CMS like system http://hep.fi.infn.it/CMS/moduletest/tkwgiu03/Zhukov-xcal.pdf

[8] V. Zhukov and W. Beaumont. *Qualification tests of Silicon strip detectors during mass production.* CMS IN-2003/041

[9] APV25 User Guide
http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/CMS/APV25-S1/pdf/User_Guide_2.2.pdf

[10] http://www-ekp.physik.uni-karlsruhe.de/ zhukov/Cms/database.html

A Fault finding algorithm

Here is the fault finding algorithm used in the analysis macro. Each step supersedes the previous ones.

1. A channel that fails any test is initially marked as an unknown problem (????).
2. If the channels is flagged as noisy in the noise test, the fault type is changed to noisy channel (NOIS).
3. If the noise and peak-time flag a pinhole and the pulse height is low, then the fault type is changed to a likely pinhole (PHL-). The channel may have been saturated, be a pinhole, have a broken preamplifier, or have a bad read/write amplifier for the pipeline.
4. Next opens are identified, in all cases the pulse height is required not to be flagged as low:
    (a) If either the noise or peak-time flags marks a one sensor open, the fault type is changed to a likely one sensor open (OSO-).
    (b) If both the noise and peak-time flags mark a one sensor open, the fault type is changed to a one sensor open (OSO+).
    (c) If either the noise or peak-time flags marks two sensor open, the fault type is changed to a likely two sensor open (TSO-).
    (d) If both the noise and peak-time flags mark an two sensor open, the fault type is changed to a two sensor open (TSO+).
    (e) If the channel is flagged noisy and the peak-time is flagged as an one or two sensor open, the fault type is changed to a likely mid-sensor open (MSO-).
    (f) Finally, if the channel is flagged as an one sensor open in either the noise or peak-time test, and a two sensor open in the other, the fault type is changes to an open of unknown location (OPN?).
5. The fault type is changed to a likely short (SHT-), if the pulse height is marked low in two adjacent channels or next-to-adjacent channels
6. The fault type is changed to a short (SHT+), if the pulse height is marked low in two adjacent channels or next-to-adjacent channels AND one of the two channels has a bad channel flag in the noise test.
7. The fault type is changed to a likely pinhole (PHL-), if the channel is flagged as a pinhole in the pinhole test.
8. The fault type is changed back to an unknown problem (????), if the channel is flagged as a pinhole in the pinhole test and as noisy in the noise test. A channel with an extremely high noise (> 10 ADC counts) can be falsely marked as a pinhole in the pinhole test.
9. Finally if a channel passes the requirements in 3) and also is marked as a pinhole in the pinhole test, the fault type is changed to a pinhole (PHL+).

B List of tests with ARC in bonding centres

We list here the sequence of operations to be done at bonding centres. The pedestal, noise and pulse shape tests must be done in all four APV modes. The pipeline test must be done only in Peak Inverter On.

First step: module arrival

First of all, perform optical inspection; then, with hybrid + PA cuts, perform:

- a complete FAST TEST
- a subset of ALL TEST: pedestal, noise, pulse shape, pipeline

Second step: HV bonding

Bond all needed HV connections, then perform, again with hybrid + PA cuts:

- an IV curve
- a complete FAST TEST
- a subset of ALL TEST: pedestal, noise, pulse shape, pipeline

Third step: strip to PA bonding

Bond sensor to PA then, using full module (1 or 2 sensors) cuts:

- perform an IV curve
- set bias at 400 V
- perform a complete FAST TEST
- perform a subset of ALL TEST: pedestal, noise, pulse shape, pipeline, led, pinhole (for this test set HV current limit to 400 μA)

Fourth step: passive cooling

The module must be cooled down to -20 °C (with no readout) and then back to room temperature. Then, using full module (1 or 2 sensors) cuts:

- perform an IV curve
- set bias at 400 V
- perform a complete FAST TEST
- perform a subset of ALL TEST: pedestal, noise, pulse shape, pipeline, led, pinhole (for this test set HV current limit to 400 μA)

Fifth step: database

Data taken after passive cooling must be written into the database. The xml is produced using the xml parser included in ARCS, taking the appropriate record from the ROOT file. All the four apv modes must be entered: peak inv on will be the REFERENCE, while all the other three modes must be flagged as VALID. All the data must be kept also in local files for future reference, and made accessible from the web.

```
Summary for module 30200020001010_400v;
Record 1
testMode: PeakOff
configFile: optimumCut_TOB_6_0.dat
Date: 2003-07-25 11:36:58.0
TestCenter: UCSB
Version: 6.0
Operator: Tony
                         ------------ -- Chip 0 -- ------------
              0000000000000000000000000000000000000000000000000000000000000000
              0000000001111111111222222222233333333334444444444555555555566666
              1234567890123456789012345678901234567890123456789012345678901234
Noise Stat    N..............................................................N
Risetime Stat ...............................................................O
Pinhole Stat  X..............................................P...............X
PulseH Stat   ................................................................
Ped Stat      ................................................................
-----------------------------------------------------------------
Summary Stat  N                                              C               D
              0000000000000000000000000000000000011111111111111111111111111111
              6666677777777777888888888899999999990000000000111111111122222222
              5678901234567890123456789012345678901234567890123456789012345678
Noise Stat    ..............................NTNO..............................
Risetime Stat ...............................T.O..............................
Pinhole Stat  ................................................................
PulseH Stat   ................................................................
Ped Stat      ................................................................
-----------------------------------------------------------------
Summary Stat                                NTNO
  Totals:
      Failed pedestal   0
         Failed noise   6
          Failed gain   0
       Failed pinhole   3   Failed pulseheight   0
      Failed risetime   3
           Test Failure Key     Channel Fault Key
   O - one sensor unbonded       O - one sensor unbonded
   T - two sensor unbonded       A - likely one sensor unbonded
   N - noisy channel             T - two sensor unbonded
   P - pinhole                   B - likely two sensor unbonded
   X - high pulse diff (PH test) P - pinhole
   G - high gain                 C - likely pinhole (saturated channel)
   J - high pedestal             D - possible mid-sensor open
   K - low pedestal              N - noisy channel
   H - high pulse height         S - short
   L - low pulse height          E - likey short
   ? - unidentified problem      F - likely open (conflicting location results)
                                 ? - unidentified problem
```

Figure 1: Example of the macro’s summary output file for one chip.

```
Bad Channel Summary for module 30200020000000; Record 6
configFile: optimumCut_TIB_6_1.dat
Date: 2003-07-07 18:02:28
TestCenter: Torino
Version: 6.0
Operator: Lino
Chan# Peak Off  Peak On  Dec Off   Dec On
2       NOIS     NOIS     NOIS      NOIS
3                         NOIS      NOIS
128     OSO-     OSO-     OSO-      OSO-
204     PHL+     PHL+     PHL+      PHL+
256     NOIS     NOIS
272     SHT+     SHT+     SHT+      SHT+
273     SHT+     SHT+     SHT+      SHT+
349     OSO-     OSO-     OSO-      MSO-
430     SHT+     SHT+     SHT+      SHT+
432     SHT+     SHT+     SHT+      SHT+
501     OSO-     OSO-     OSO-      MSO-
510                       NOIS      NOIS
511     NOIS     NOIS     NOIS      NOIS
Channel Fault Key
OSO+ :one sensor unbonded (confirmed by two test)
OSO- :likely one sensor unbonded (only seen in one test)
TSO+ :two sensor unbonded (confirmed by two test)
TSO- :likely two sensor unbonded(only seen in one test)
PHL+ :pinhole (confirmed by all possible tests)
PHL- :likely pinhole (saturated channel)
MSO- :possible mid-sensor open
NOIS :noisy channel
SHT+ :short(low pulse shape + 1 at least one channel weird
noise
SHT- :likey short (only low pulse shape)
OPN? :likely open (conflicting location results)
???? :unidentified problem
```

Figure 2: Example of the macro’s bad channel list output.

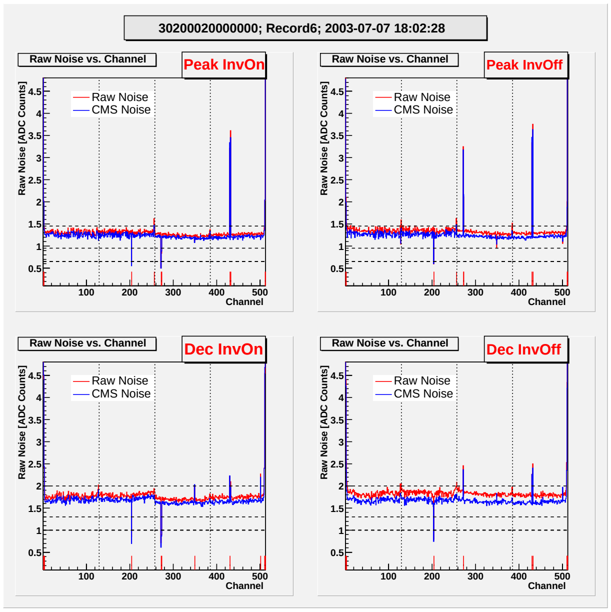

Figure 3: Example of noise (in ADC counts) for each channel in each mode for a TIB module. Cut values (for TIB) are displayed as horizontal dashed lines (vertical dashed lines represent chip boundaries). Red marks at the bottom of the plot indicate which channels failed.

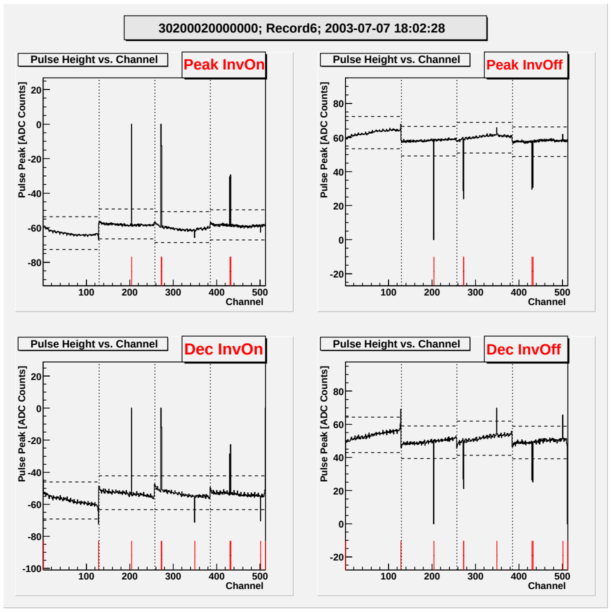

Figure 4: Example of pulse amplitude (in ADC counts) for each channel in each mode for a TIB module. Cut values (for TIB) are displayed as horizontal dashed lines (vertical dashed lines represent chip boundaries). Red marks at the bottom of the plot indicate which channels failed.

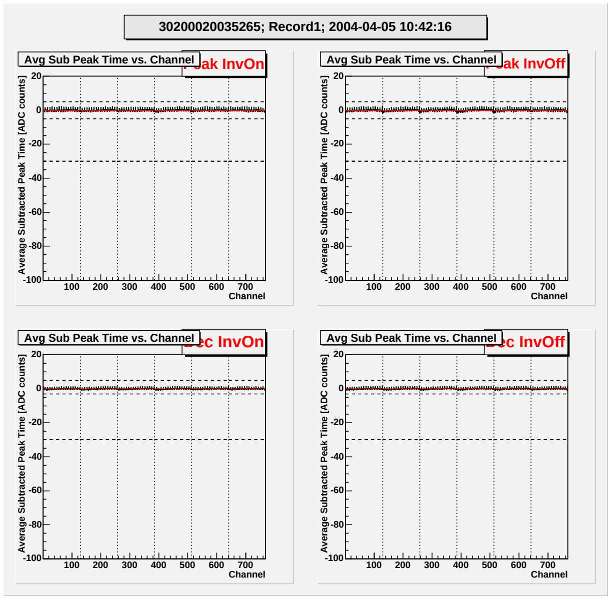

Figure 5: Example of average subtracted peaktime (in nanoseconds) for each channel in each mode for a TIB module. Cut values (for TIB) are displayed as horizontal dashed lines (vertical dashed lines represent chip boundaries). Red marks at the bottom of the plot indicate which channels failed.

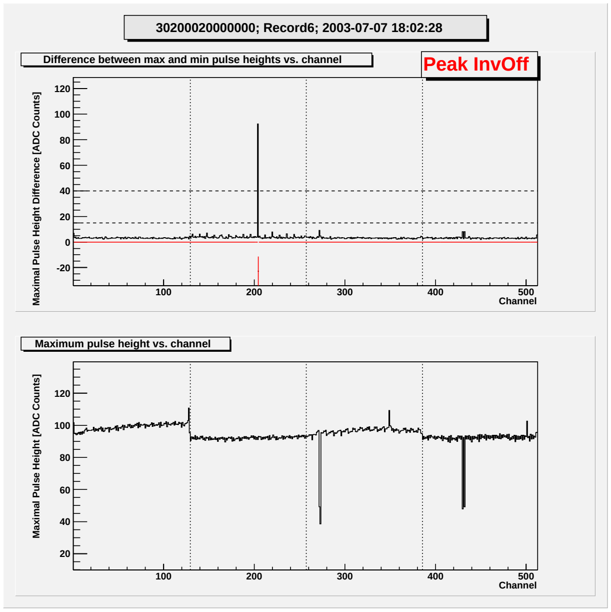

Figure 6: Examples of the maximum differences in calibration results (in ADC counts) for each channel in Peak Inverter Off for a TIB module. Cut value (for TIB) is displayed as horizontal dashed lines (vertical dashed lines represent chip boundaries). Red marks at the bottom of the plot indicate which channels failed.