

ARCS Status Report





**Module Test Meeting
CMS Week
25th February 2003**

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Last Tracker Week:

- Pinholes created by LED Test? 
- Special Database Meeting on Module Tests 
(S.Perries, V.Zhukov, M.Meschini,)
- Talk of A.Affolder on experience from CDF 
- C.Civinini talk on Edge Channel Noise 

Creation of Pinholes by LED Test

- Two new pinholes were found on a module
- No idea how they were created

Does the pinhole test create pinholes?

Module with Hybrid 30216630200101:

- One pinhole + one high leakage current pinhole

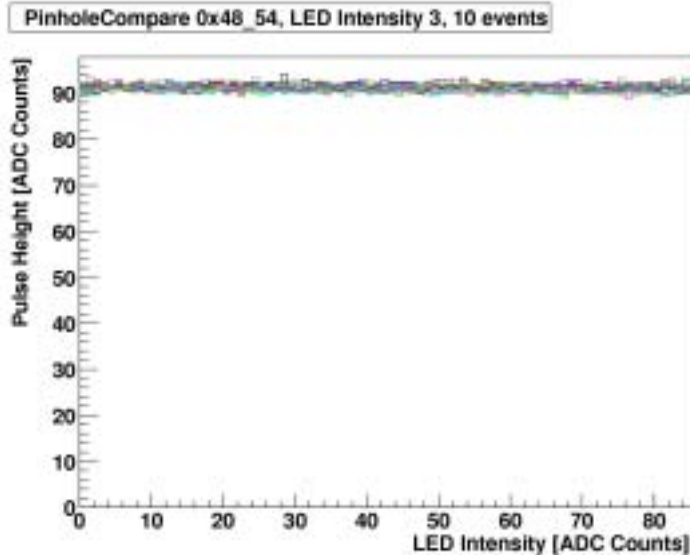
Testprocedure:

- 25 automated pinhole test cycles
 - Continuously irradiated the sensors with light from LEDs
 - Applied calibration pulse
 - Measured maximum signal height
 - Increased LED intensity

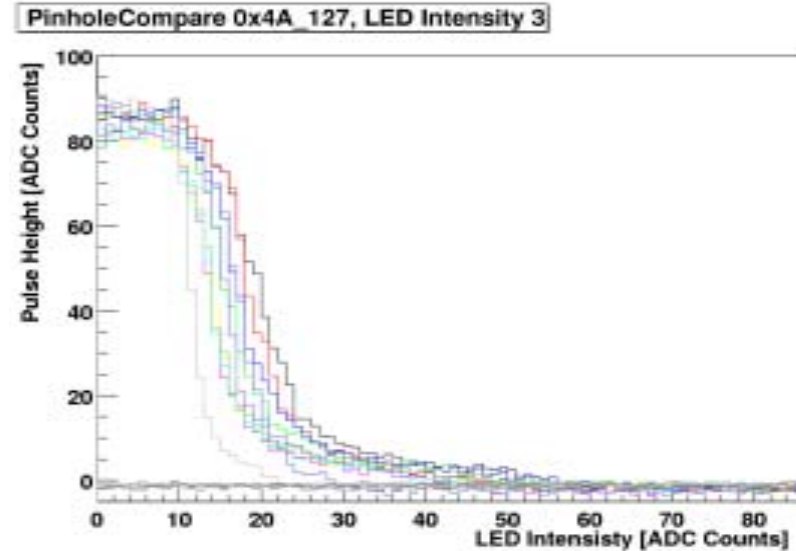
→ Filled maximum signal in ADC counts into a histogram

Creation of Pinholes by LED Test

Working channel



Channel with pinhole



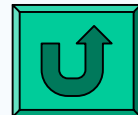
- No additional pinholes occurred after 25 runs
- Working channels did not change their response to calibration pulses
- One pinhole showed time dependent behaviour



pinhole test did not create additional pinholes



more tests are needed to be sure



Discussed new xml template:

(V.Zhukov put it on the web; implemented in test DB)

- **Reduced complexity**
 - One basic action Modvalidation
 - Environment variables filled in once
- **Reduced size**
 - Pedestals, noise, calibration amplitude just stored for one APV mode
 - Tests in other modes are reported by bad channel flags
- **All of our questions were answered**
 - We can go ahead for a first final version



Everything is fine for us but some changes in ARCS have to be done!

Necessary changes in xml parser:

- Use V.Zhukovs Qt based xml parser
 - **Problem:**
 - (Qt development kit for windows costs 1500€ per developer)
 - **Solution:**
 - xml parser based on xerces-c2_1_0-win32
 - Parser is available
 - Creation of xml files with new structure no problem

Necessary changes in root file structure:

Previous ARCS versions:

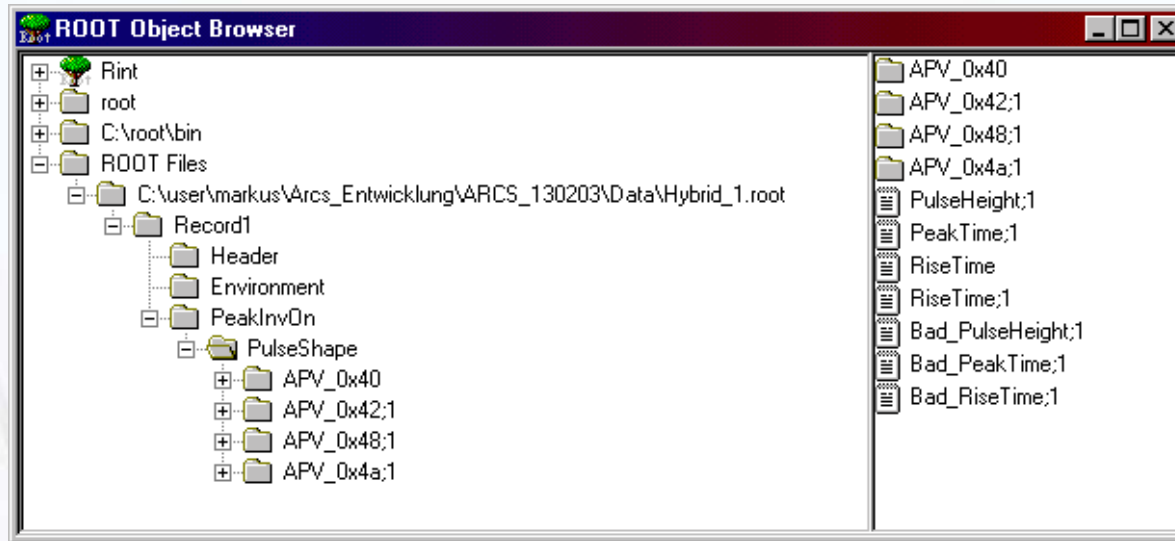
- One root file for every single test
 - Many files
 - Not nice to handle
 - More work on parser
 - Deal with many files
 - High probability of errors

➔ Root file organisation had to be changed!

New ARCS version

- Just one root file is created for every test object
 - Less number of files
 - Easy to handle
 - Allows clear arrangement of data

Example of new root structure:



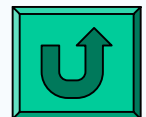
- Clear arrangement of data
- Possibility to do as many test as you like
- APV modi indicated in sub folder name
- Contains all important information
- Changes in xml template can easily be handled by parser

Structure should be seen as an approach to final version!

➔ If you propose changes let us now!

New ARCS release:

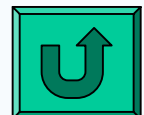
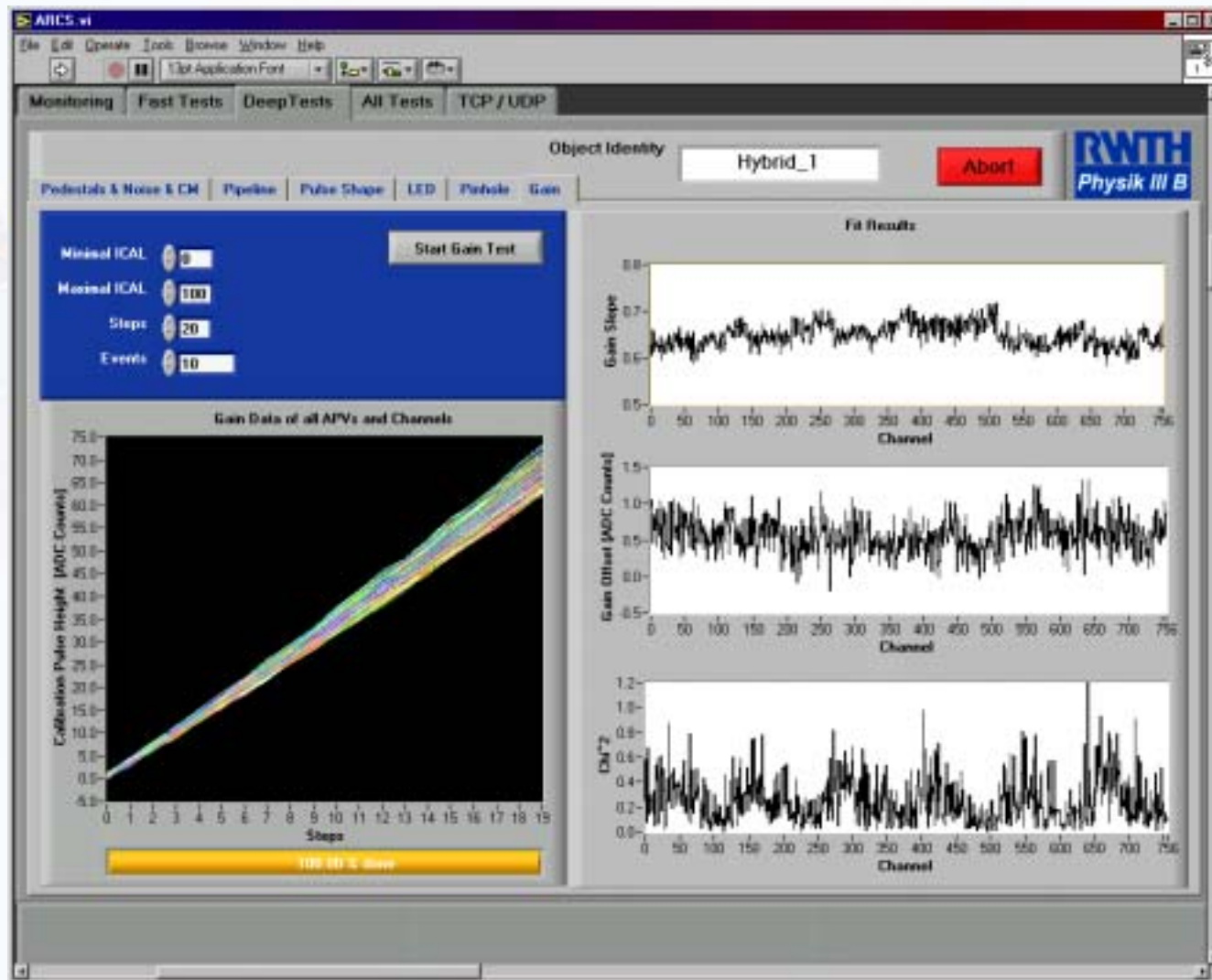
- All changes are implemented
- Release date next week
- At present tests are done to find bugs



A. Affolder proposed to have a closer look
at APV

gain

- Implemented a gain test in ARCS
 - Take pulse shape to find maximum signal height
 - Apply different amount of charge by changing ICAL
 - Create plot signal height over ICAL setting
 - Apply linear fit to get offset and slope



C.Civinini:

Tested tib module to see influence of additional capacitor on edge channel noise

- Noise reduced
- Common mode is also reduced

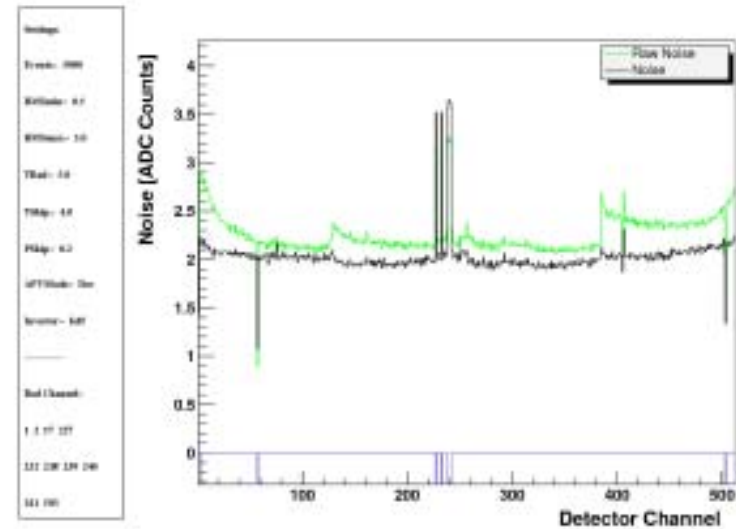
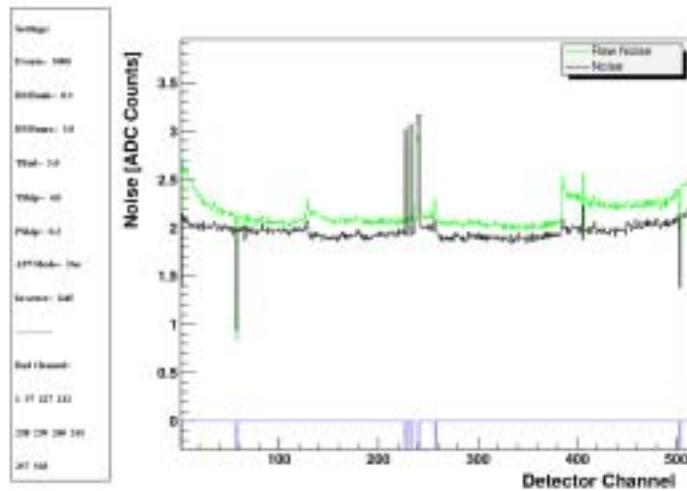
Redid test with tec module 30216711300238
(latest version of tec modules)

1. Take pedestals, noise, pulshape..
2. Add capacitor on hybrid with 33pf
3. Redo measurements
4. Compare results

Deconvolution Inverter off

With Capacitor to ground

Without Capacitor to ground

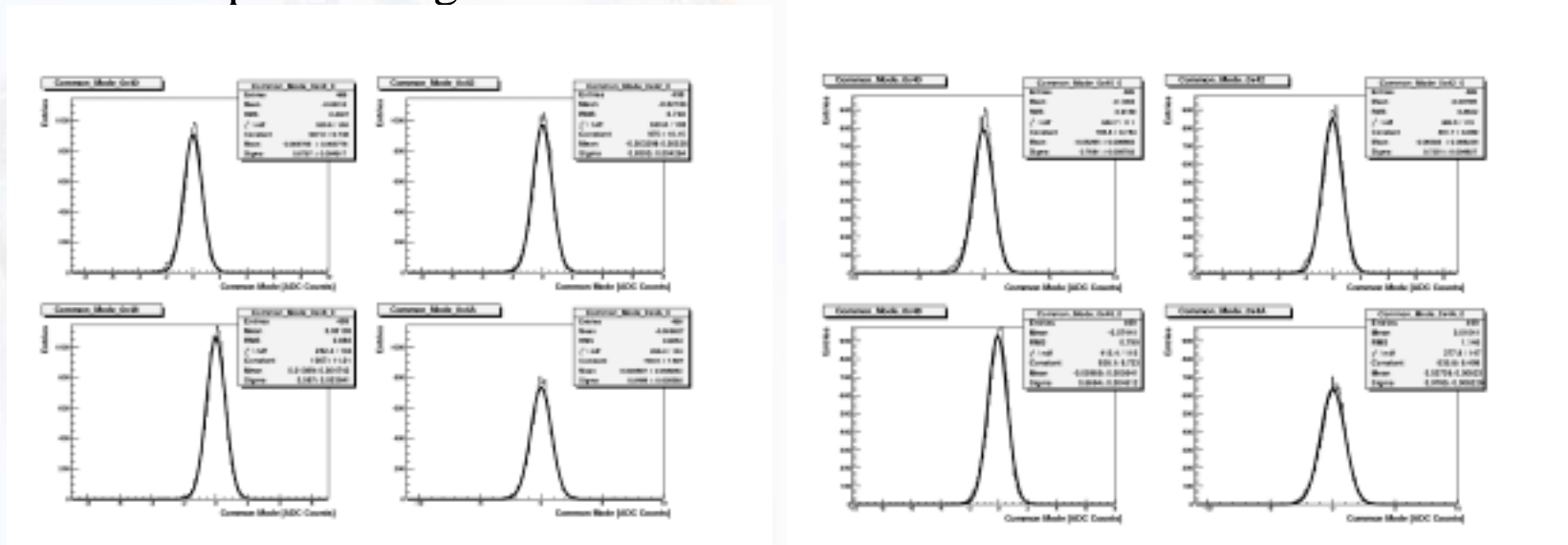


Noise at the edges is slightly lower when capacitor is added

Deconvolution Inverter off

With Capacitor to ground

Without Capacitor to ground



Common mode is also reduced when capacitor is added

➔ **Measurements are consistent with Carlos results!**

