



0V.

Deep In TIB Production Results

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Module Test Meeting

Tracker Week

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UV.



Module Test Status

- 6 centers involved in production modules testing: Bari, Catania, Firenze, Padova, Pisa, Torino
 - All the centers are bonding and ARC testing
 - All centers but Bari have started LT tests
- More than **200** modules bonded and ARC tested
- More than **50** modules LT tested
- The overall quality of modules is good
- New testing procedures are in place in pilot centers; testing is now much faster
 - We have chosen to stop the passive cooling cycle if no new problem arise



Module Test Status (II)



	Received	Bonded	ARC Tested	Good modules	LT Tested
Bari	33	23	21	19	0
Catania	25	10	9	9	6
Firenze	35	35	35	35	26
Padova	48	28	28	26	6
Pisa	100	94	94	91	30
Torino	36	36	36	36	6
Total	277	226	223	216	68

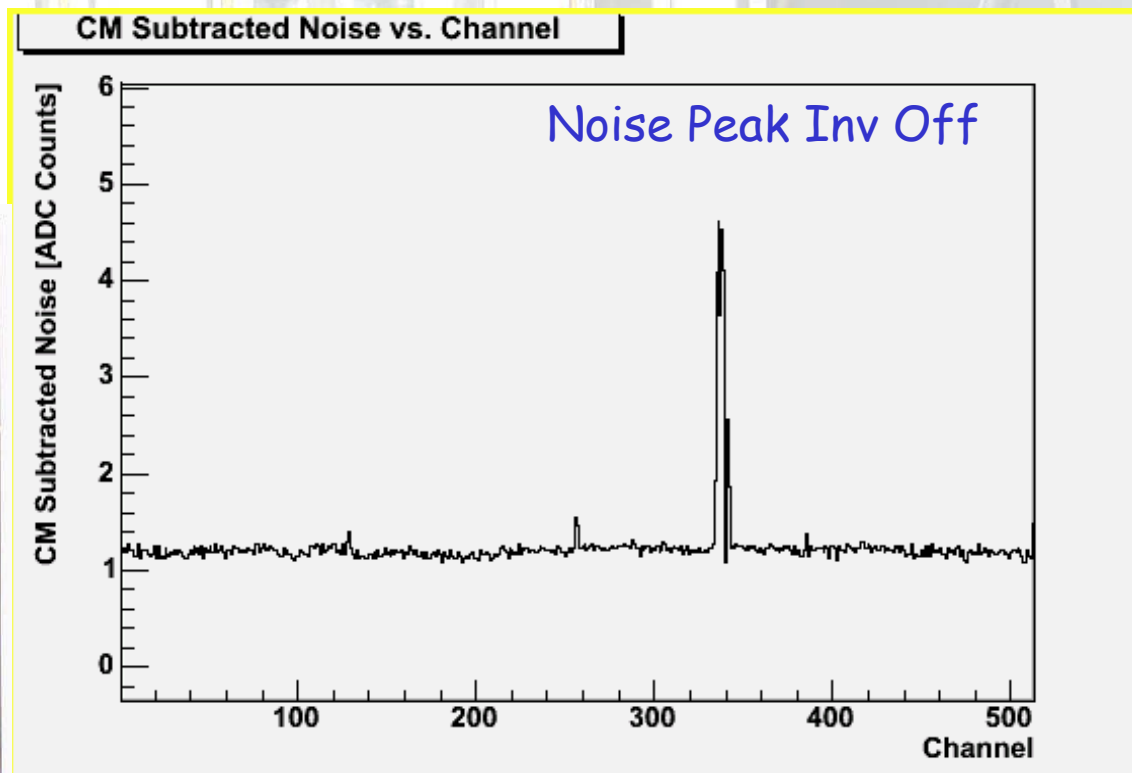
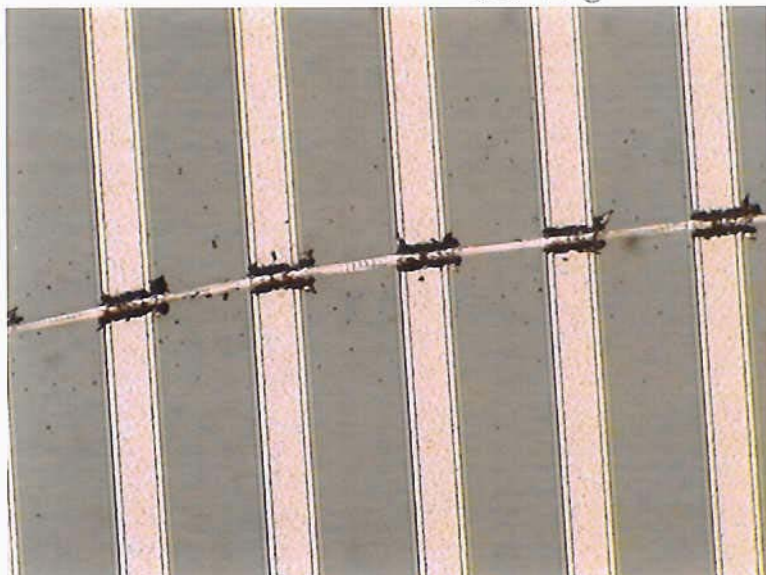


ARC Results



- On a total of more than 200 modules tested, we found **7** bad modules:
 - 2 have been tagged for bad strips number ($>2\%$)

A short of 9 channels: scratch on the silicon crystal shorting the strips



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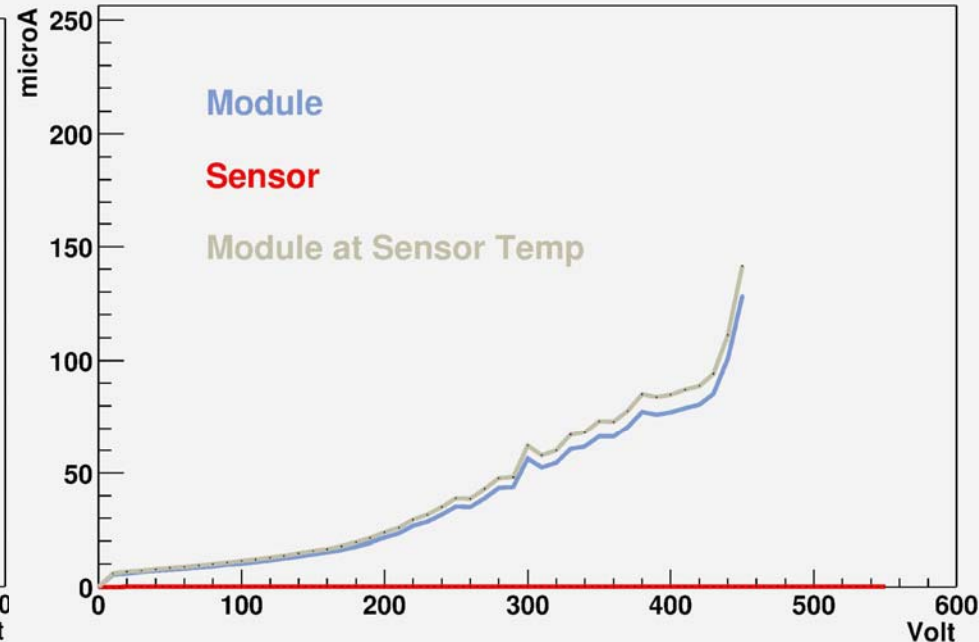
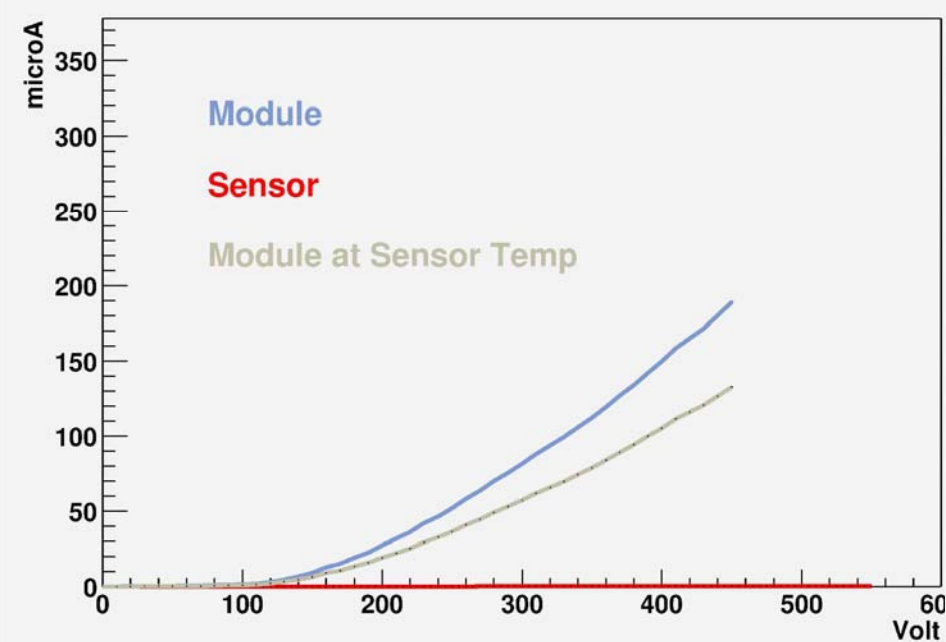
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IV Curves



- 4 of them have been flagged as bad for IV problems
- Two modules with a bad IV behaviour after bonding
- Both sensors showed no problem in sensor DB



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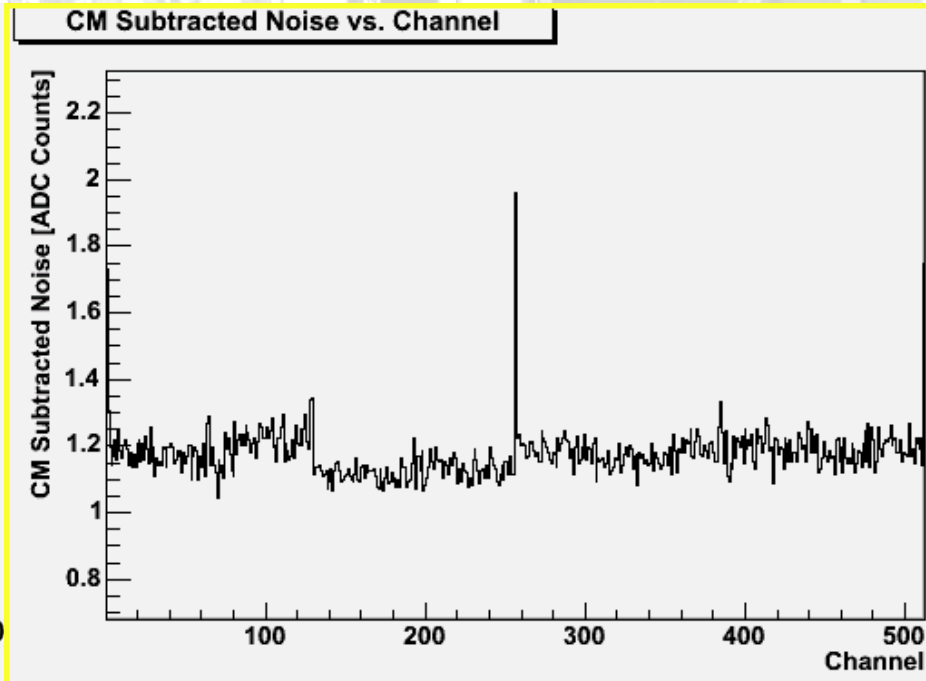
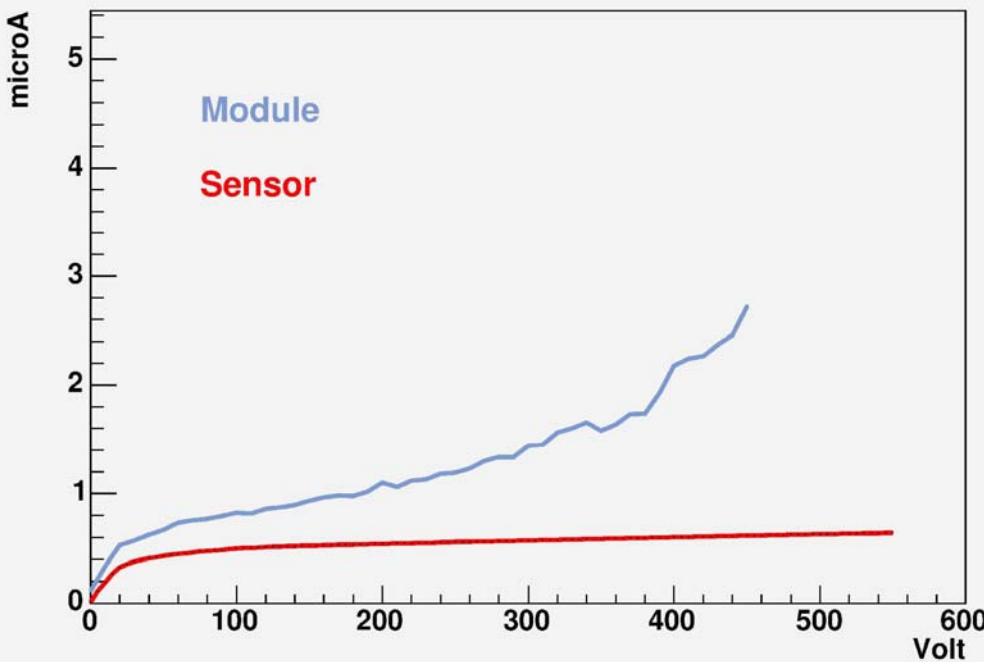


IV Curves (II)



- There are also modules that after bonding have a high current with respect to the other TIB modules, but below the $10\ \mu\text{A}$ cut
- All these modules result good in all the other tests

→ They are considered GOOD





LT Results



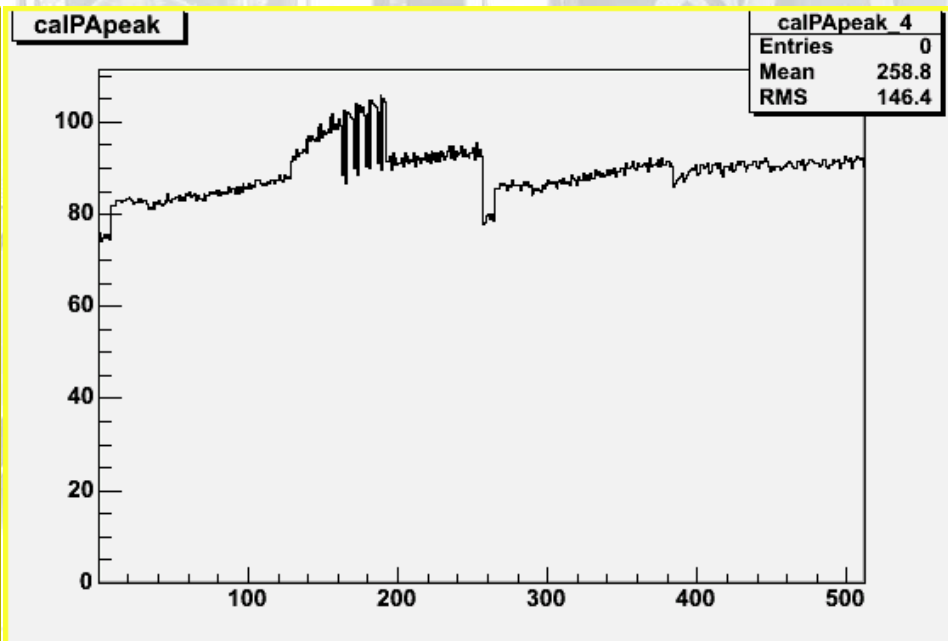
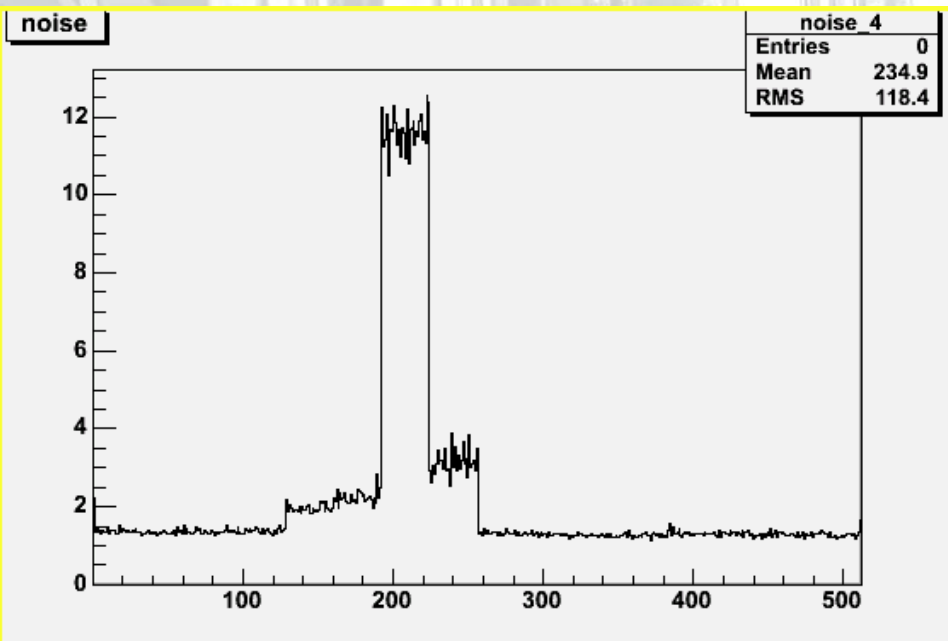
- LT Version 1.22 is used everywhere in TIB community
 - Padova, Catania, Torino and Firenze are running with 6 modules at a time
 - Pisa is running with only 4 modules at a time
- The LT software has still some stability problems running a 72 hours scenario
- We lose some modules after some cooling cycles
- We are investigating in collaboration with Wim on the causes of these problems
- Up to now **10** modules have failed in LT tests



LT Results (II)



- 1 module broken during thermal cycles
 - We tested again this module with ARCS at room temperature and there are problems with the I²C communication
 - Nothing strange is visible in an optical inspection
- It's possible that cooling cycles induced some connection problems on this module



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LT Results (III)

- 9 more modules have shown some problems, mostly at low temperature:
 - mainMonitor stops to acquire data from those modules, usually due to a high number of pll errors
 - No evident correlation with hybrids tested at CERN at low temperature that showed pll problems
- Retesting them not always shows modules problems
- We are still investigating if these modules are really broken or if they can be recovered



LT Test Settings

- We are using a common **settings file** and a common **scenario** in all the TIB centers
- Our scenario is composed by 9 cooling cycles between 20°C and -20°C , over 72 hours:
 - At -20°C we do a full set of measurements (pedestals, calibration and IV in all the APV modes)
 - At 20°C we do a shorter test (pedestals and calibration in peak inverter on)
 - In 3 warm points (first, last and in the middle of the scenario) we do a full set of measurements



LT Test Settings (II)

- After the first "official" LT runs, we have fine tuned some settings
 - A module is excluded from acquisition if it reaches a maximum error number. To solve some stability issues, we have chosen to set this value to 1000.
 - This doesn't solve all the problems
 - Wim informed
 - We have implemented the new cuts (see Riccardo's talk) in the settings.xml file
 - Calibration amplitude has been set to 2 MIPs



LT Test Settings (III)

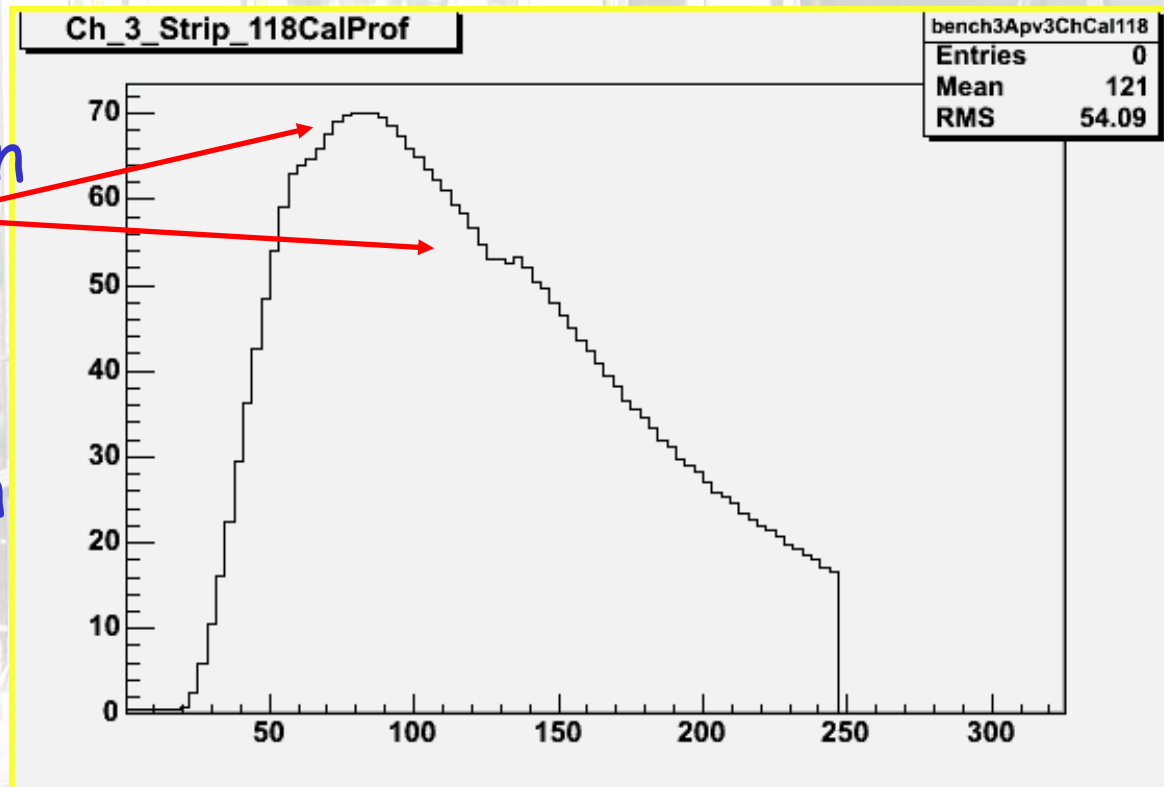
- We have chosen to evaluate the maximum of the calibration pulse using the same routine as ARCS
- The baseline level has been adjusted for every mode of the APVs to be well within the digital 0 and digital 1 when in calibration mode
- An init sequence is sent to the pll before each measurement step, both at cold and warm temperature
- The APVs are switched off (Hard Reset + analog off via I²C) for one hour two times at -20°C
 - This scenario has been tested only in Florence yet
 - You can find it at <http://hep.fi.infn.it/CMS/marchett>



LT Calibration



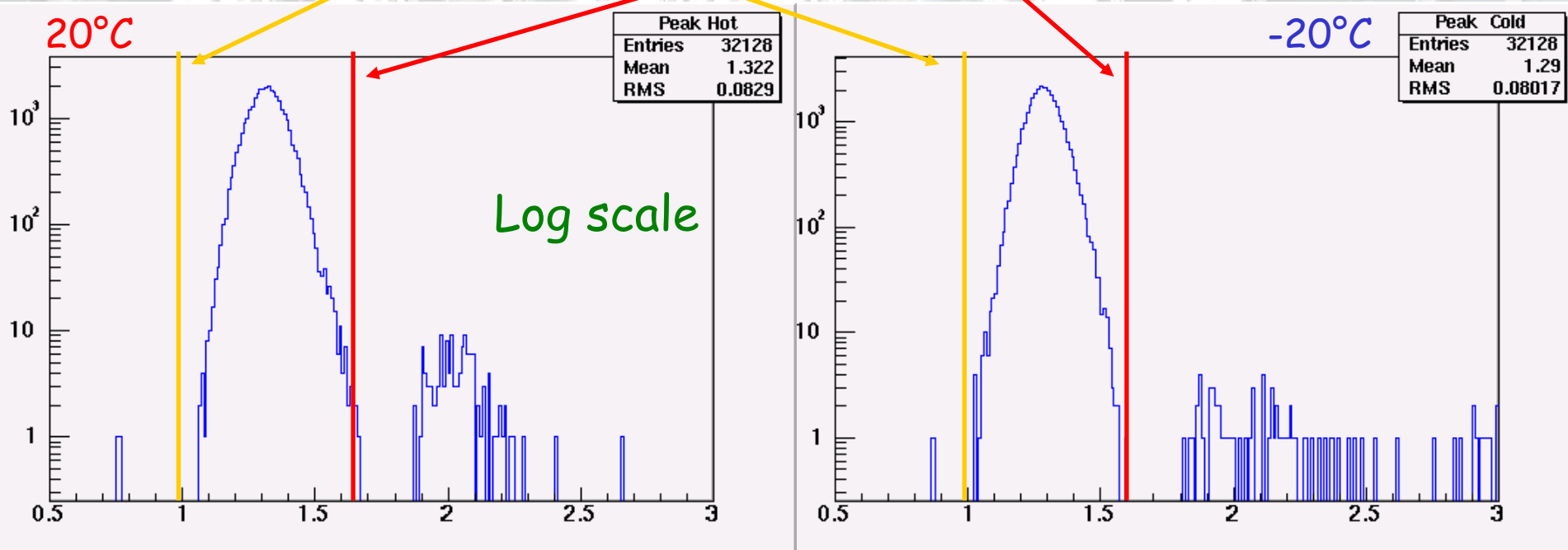
- Strange behaviour in calibration pulse, **observed at least in Firenze, Catania and Pisa**
- This effect is not observed in ARCS
- There is a double peak in calibration profile in peak mode
- This can produce strange results in the fit of the peak height





New LT Cuts

- Example of new LT cuts
- Chip edges are not included in these plots
- Peak mode: $1.00 < \text{healthy} < 1.65$



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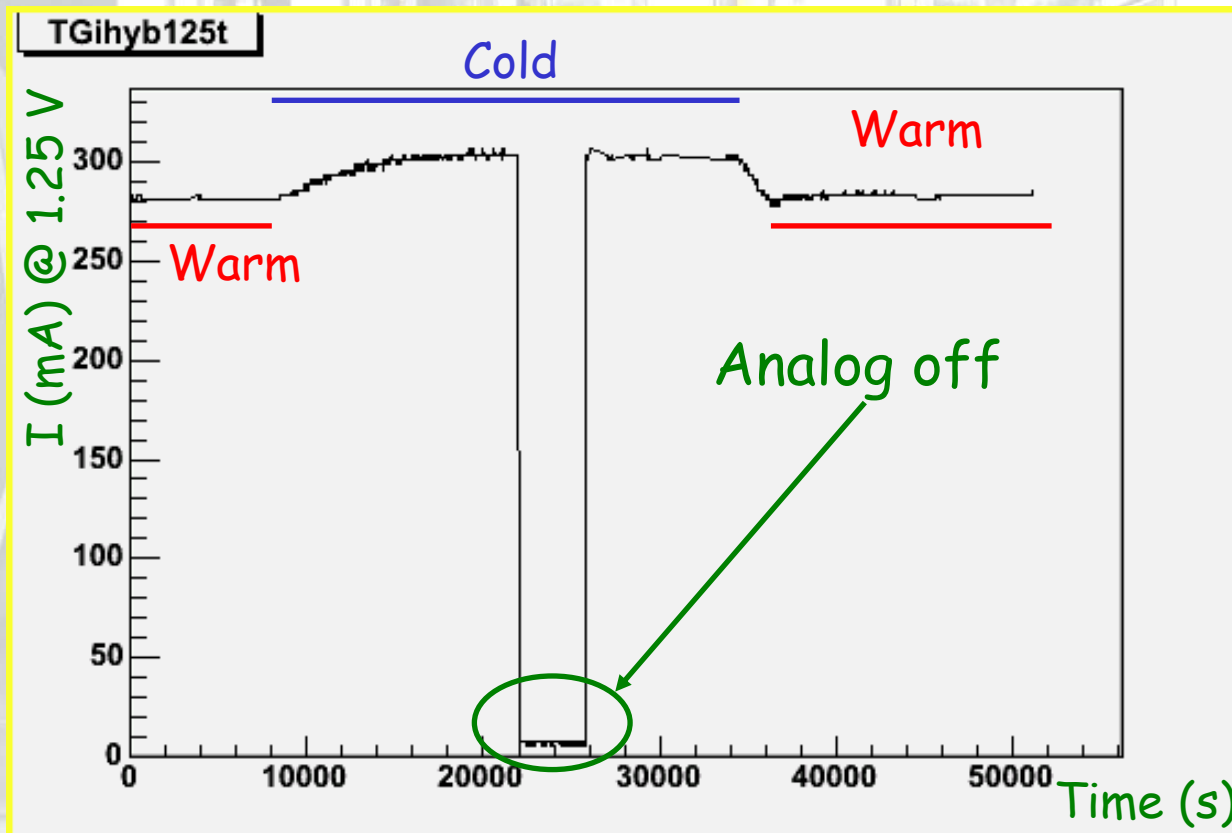
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LV Currents @ 1.25 V



- With the new settings, we really switch the APVs off
- This can be observed looking at the LV currents

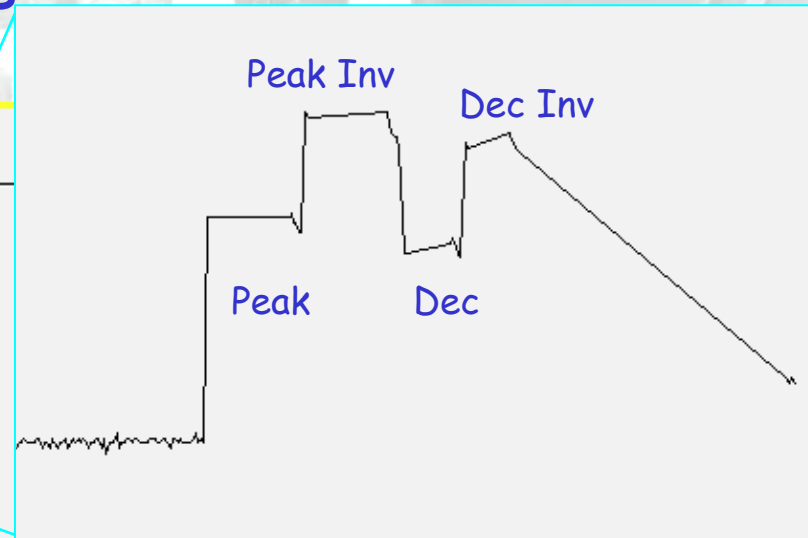
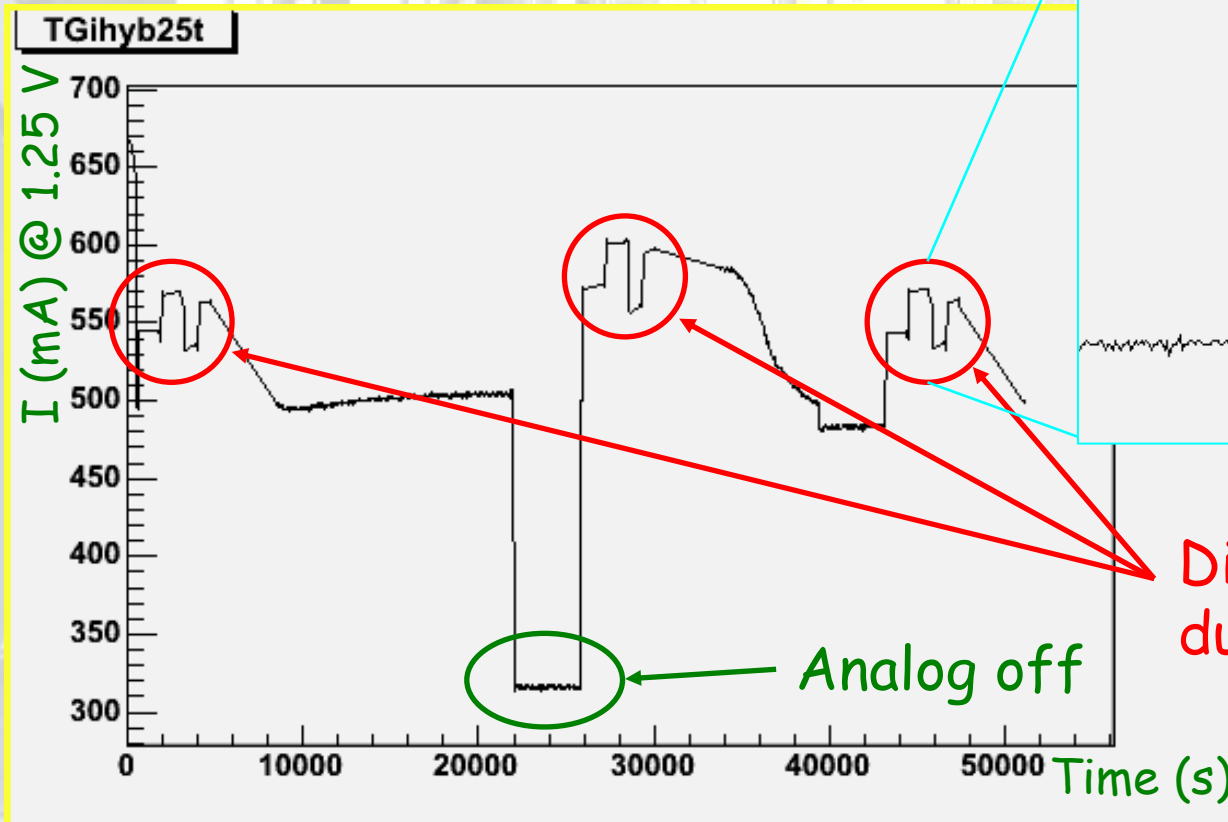


Measurements taken with Wim's PAACBs



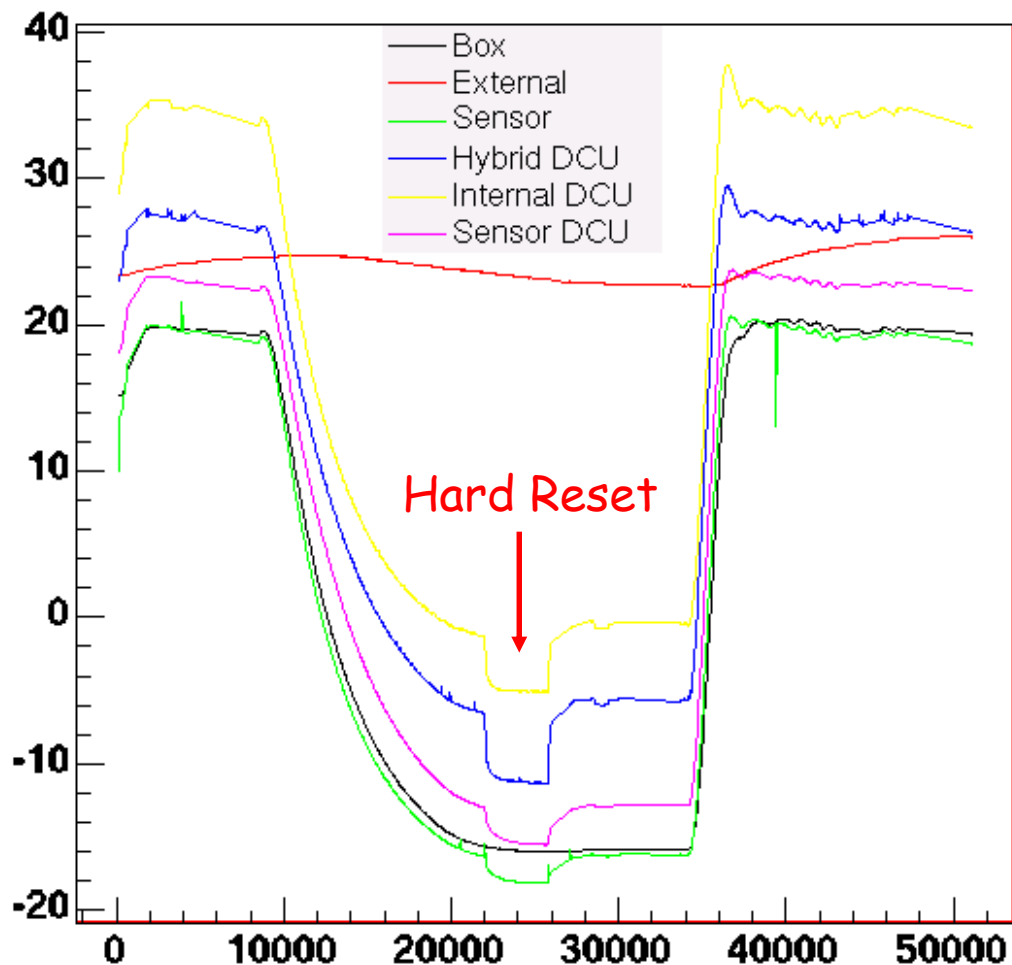
LV Currents @ 2.5 V

- In the 2.5 V current we can see the different consumption in different modes



Different baseline values during measurements

- All the centers reach almost the same temperatures on hybrid and silicon
- The silicon temperature goes down to -15°C
- The hybrid temperature reaches -10°C





LTXML



- There are still differences with respect to the ARC version (**chflag**)
- Some fields are not filled (**CMN**) or are wrongly filled (**average noise**)
- The calibration cut is an absolute cut while we chose a percentage one
- Up to now it's impossible to produce an output usable for the database



Conclusions

It could be worse...



The True Conclusions

- All the centers involved in production are bonding and testing modules with a good speed, but we have to increase the weekly rate
- LT is not yet started in all the TIB centers
- With more than 200 modules bonded and tested we can say that:
- Up to now the overall quality of TIB modules appears to be good
- Still some problem on LT tests, we are working with Wim to find a solution



The True Conclusions (II)

- We have **223** modules ARCS tested and **68** LT tested
- There are:
 - 7** really bad modules → **3 %**
- Taking into account also the suspicious modules:
 - 17** bad modules → **8 %**