CMS Module Testing Issues

From a CDF Testing Experience Perspective

Anthony Affolder
(for the UCSB module testing group)

Talk Overview

- Review current CMS testing procedures
- Assorted observations from our limited testing experience on CMS components
- UCSB module testing
  - Personnel, equipment, and infrastructure

CMS Testing Overview

- Review of current CMS testing procedures
  - Ensure understanding of testing prior to arrival at FNAL/UCSB
    - Reproduction of all faults, etc.
  - Make sure any systematic failures in production techniques/materials found as early as possible
    - M800 pre-production first chance to produce large quantities of single type of modules
    - Need to be able to track time development of faults
- Responsible to aid in answering open questions before large scale production
  - Need of burn-in of module/optical systems components
  - Finalization of production procedure
  - Finalization of testing procedure
    - Both fault finding and module qualification

Tests Prior to Arrival at FNAL/UCSB

- APV Chip Testing (1 minute)
  - Voltage stressing (6 sec)
  - Basic Functionality
    - Pedestal
    - Calibration Injection (2 MIP)
    - Pipeline
- FHIT-Industrial Testing (1 minute)
  - Connectivity
  - Basic Functionality
    - Pedestal
    - Calibration Injection (2 MIP)
    - Noise
- Strasbourg
  - ?????
- CERN-Pitch adaptor bonding (20 minutes)
  - Basic functionality
    - Pedestal
    - Noise
    - Calibration Injection (2 MIP)
  - Capacitive pulsing pitch adaptor
  - Thermal cycle to –20 C
    - Repeat test
  - Warm to room temperature
    - Repeat test

Testing Concerns

- Hybrid tested ~1-20 minutes prior to arrival at FNAL/UCSB
  - Leads to concerns about infant mortality problems
  - CDF Hybrid Burn-in Experience
    - 4 days with extensive tests at start/end

      + 3 Day of Module burn-in
    - ~9 out of 8000 chips failed (0.1% of chips)
    - Same rate would lead to 2%(5%) rework of rod
- Optical hybrids also will not be burnt-in
  - CDF optical hybrid experience
    - 3 day burn-in with tests at beginning and end
    - ~10% failed during burn-in (soft number)
    - Additional 9 DOIM (out of 556) failed during data-taking

      CDF used custom laser diode system

Testing Concerns (2)

- Some components of hybrid characterization can be made stronger
  - Test calibration circuit at multiple injection points
  - Test pipeline pedestal/noise with larger statistics
    - CDF calibrations remove bad cells from noise/pedestal calculation
  - Suggest such test done prior to pitch adaptor bonding
- Testing requirements can be made more consistent between sites
  - Pedestal requirement change between test stands
  - On-chip common mode subtraction “feature” makes noise characteristics of open/saturated channels unpredictable
  - Common-mode subtraction also different between stands
- Recent hybrid circuit modifications change LED pinhole tests characteristics

Common-mode Subtraction

- Differing algorithms used to calculate common mode pedestal for subtraction
  - ARC
    - 4 groups of 32 channels per chip
    - Use average as common mode for each section
  - DAQ
    - Strips (after subtracting the channel's average pedestal) are ordered with highest/lowest 10% truncated
    - Use average of remaining strip as common mode for chip
  - Final FED
    - Median channel value (after pedestal subtraction) is used as common mode
- Use of same algorithms will yield more uniform testing/qualification results between stands

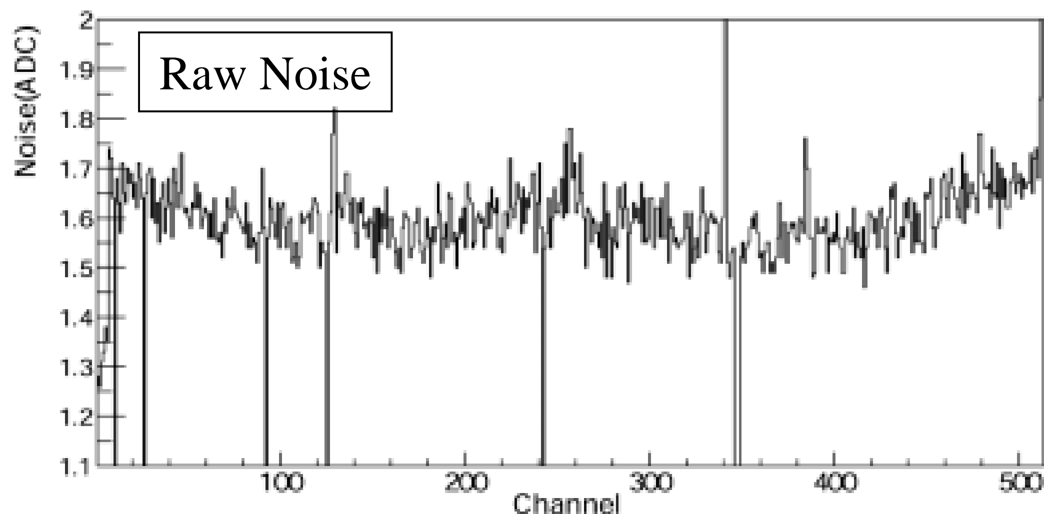
Test System Grounding Issues

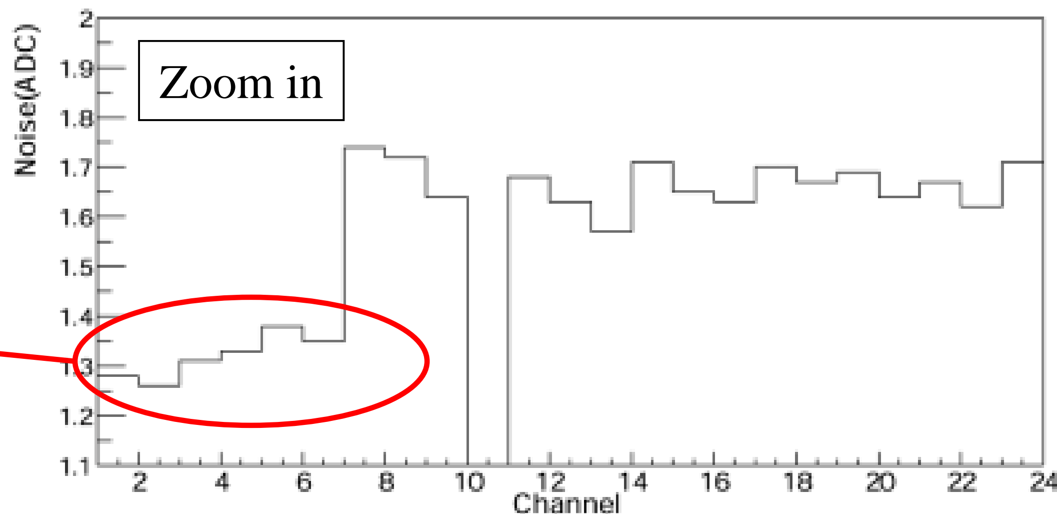
- PC, DAQ/ARC, LV supplies, and HV supply share common ground
  - Can lead to less than predictable test results
    - See frequency related noise of prototype rod tests (D. Abbaneo)
- Suggest that a common mode noise standard is made
  - With inverter off in peak mode (~0.5 ADC)
    - Removes on-chip common mode "feature"
  - Allows for more uniform testing results

Lower Noise Requirements

Improving grounding until common mode noise less than ~0.5 ADC in peak mode/ inverter off allows the use of raw noise as a powerful tool for finding opens, including the location

- Sensor-Sensor
- Pitch Adaptor-Sensor
- APV-Pitch Adaptor (???)
  - ✓ Seen by Charge Injection

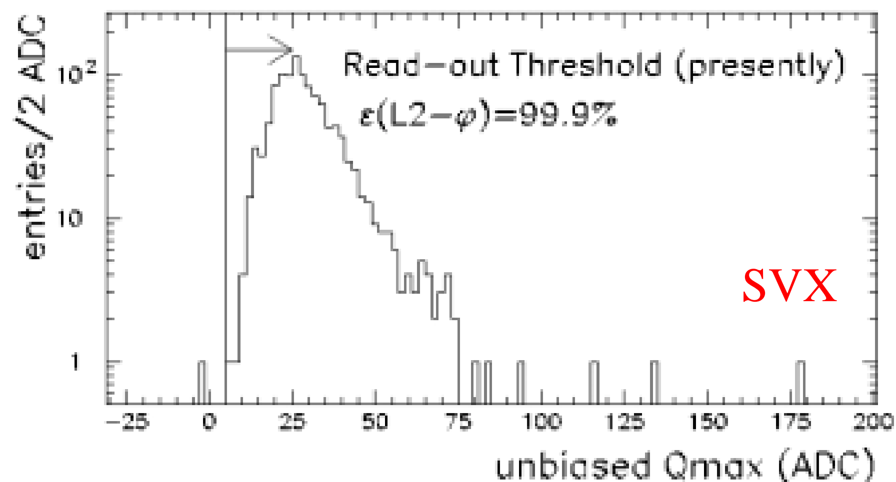


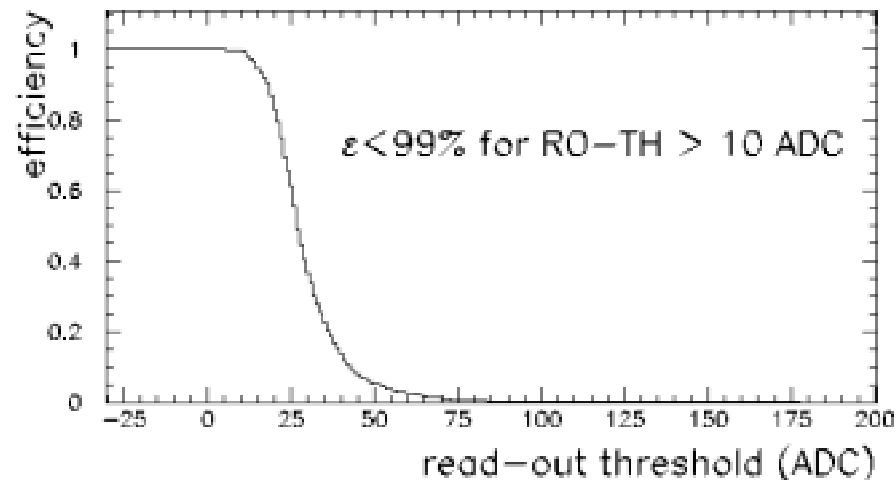


Sensor-Sensor Open Visible

Upper Noise Requirements

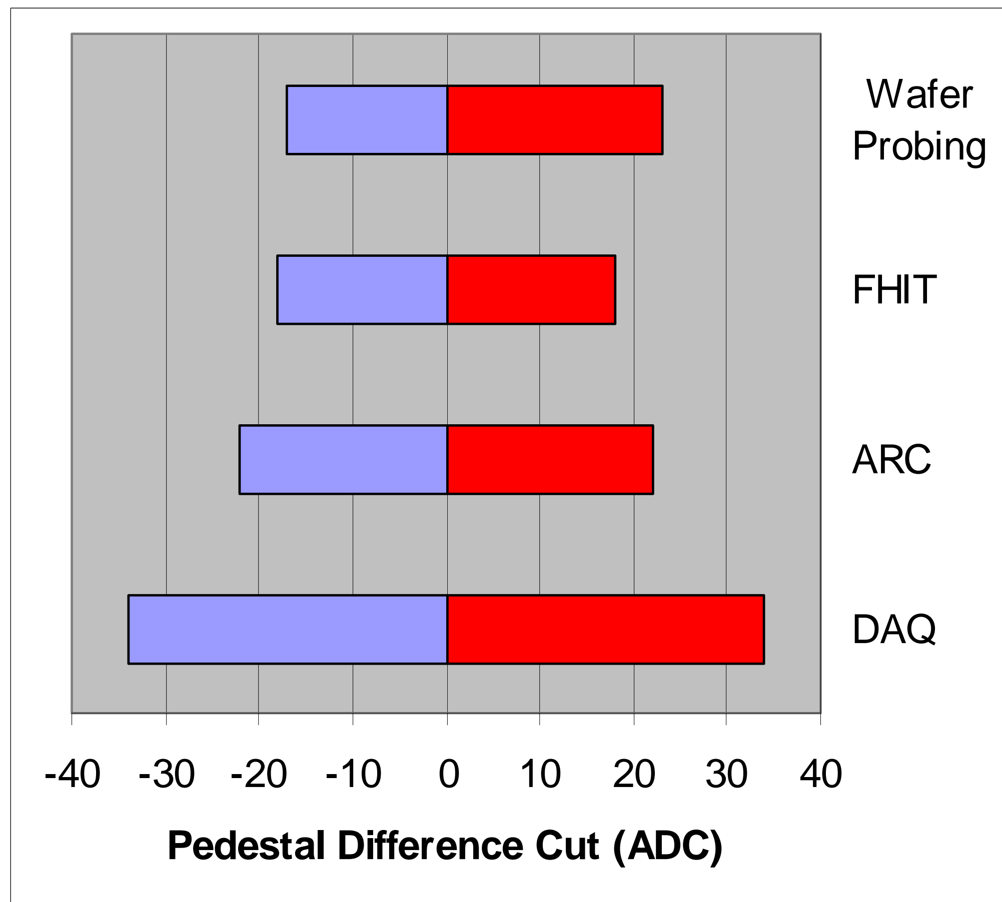
- High noise only affects signal efficiency (clustering)
- Use physics (radioactive sources/comic ray stands/collision data) to determine cut value
  - Expect values to be different for different systems
- Wider Cut Values





Pedestal Tests (Current)

- Wafer Probing
  - Dynamic Range: 0-240 ADC
  - Average Pedestal: 67.1
    - 50 <P < 90 ADC Cut
- FHIT (Industrial Tester)
  - Dynamic Range:0-240 ADC
  - Average Pedestal:~90
- ±20% Cut:~72<P<108
- ARC
  - Dynamic Range:0-240 ADC
  - Average Pedestal:~110
    - ±20% Cut:~88<P<132
- DAQ
  - Dynamic Range:140-380 ADC
  - Average Pedestal:~170
    - ±20% Cut:~146<P<194



Pedestal Requirement vary by as much as 70%

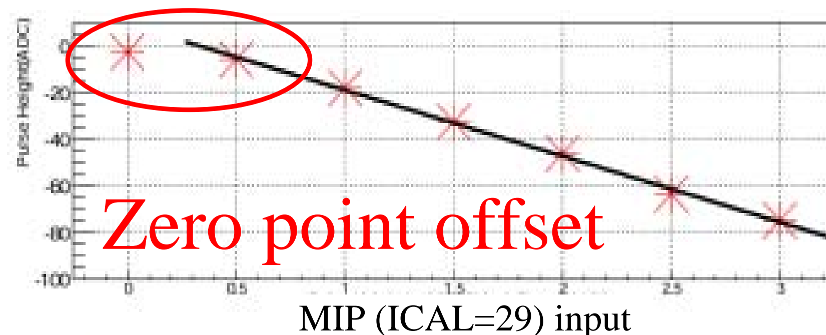
Suggested Pedestal Tests

- Pedestal variation only effects dynamic range of channel's pre-amp or may indicate pathological problem
  - Suggest defining pedestal requirements in similar manner as in wafer probing
    - In wafer probing, absolute pedestal requirements with a given width relative to the mean of the test stand

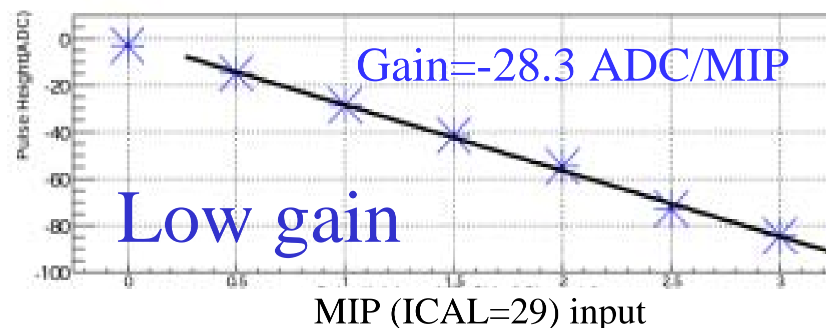
Gain Measurements

- Single point gain does not tell full story
- Convolution of front-end w/ calibration circuit
- Is there a physics based gain spec?

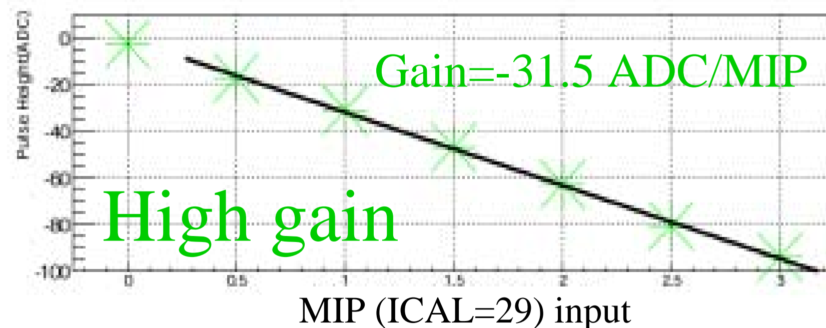
Extreme cases seen:



MIP (ICAL=29) input



MIP (ICAL=29) input

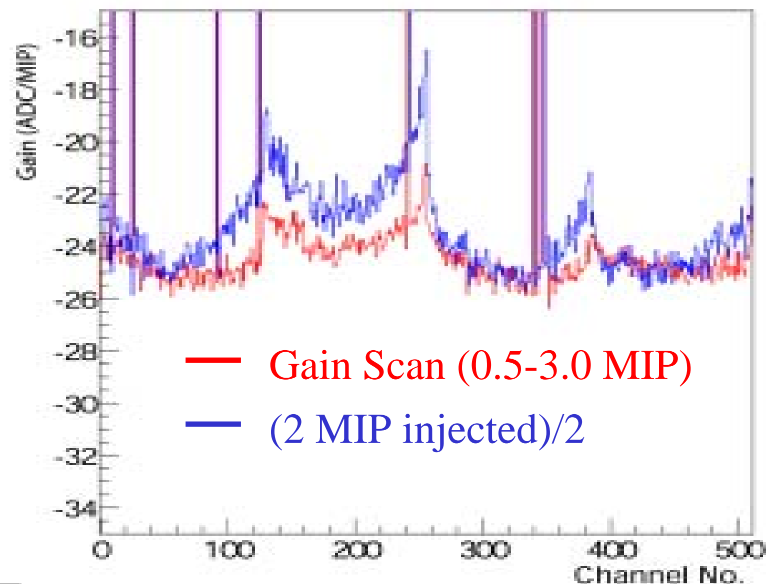


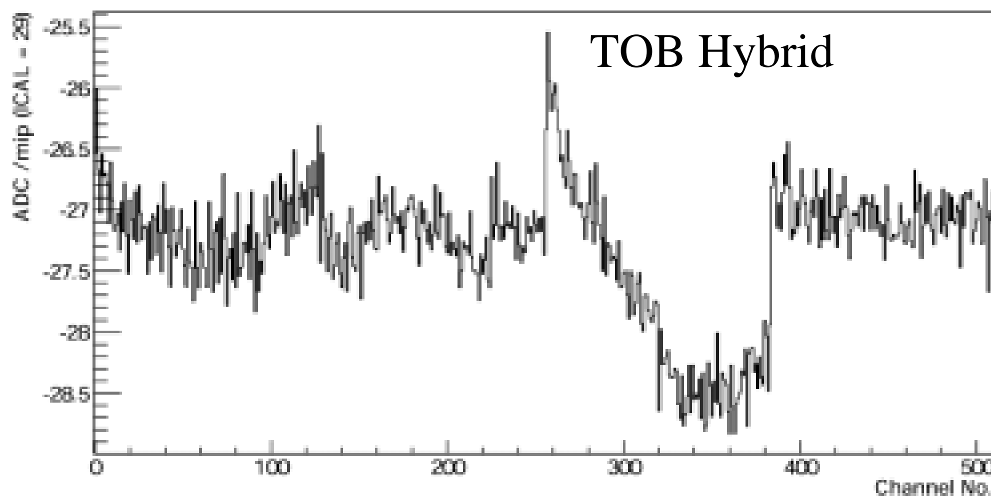
MIP (ICAL=29) input

Gain Measurements (2)

- Multi-point gain measurements have many advantages
  - More stable
  - More uniform between chips
    - Tighter Cuts

TOB Module 83

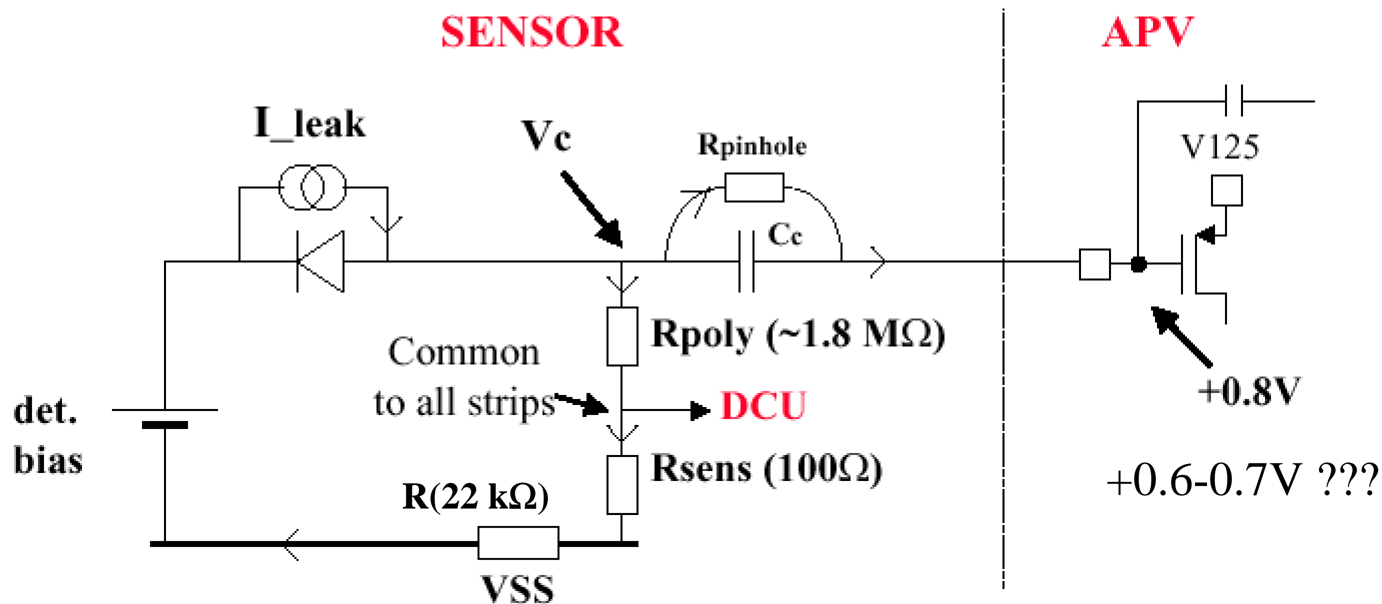




- Shows non-linearities
  - Zero MIP injection
- Shows non-uniformities within chip
- Calibration very sensitive to environment
- Easy to implement

LED Pinhole Test

- LED pinhole test characteristics will change with bias return line modification

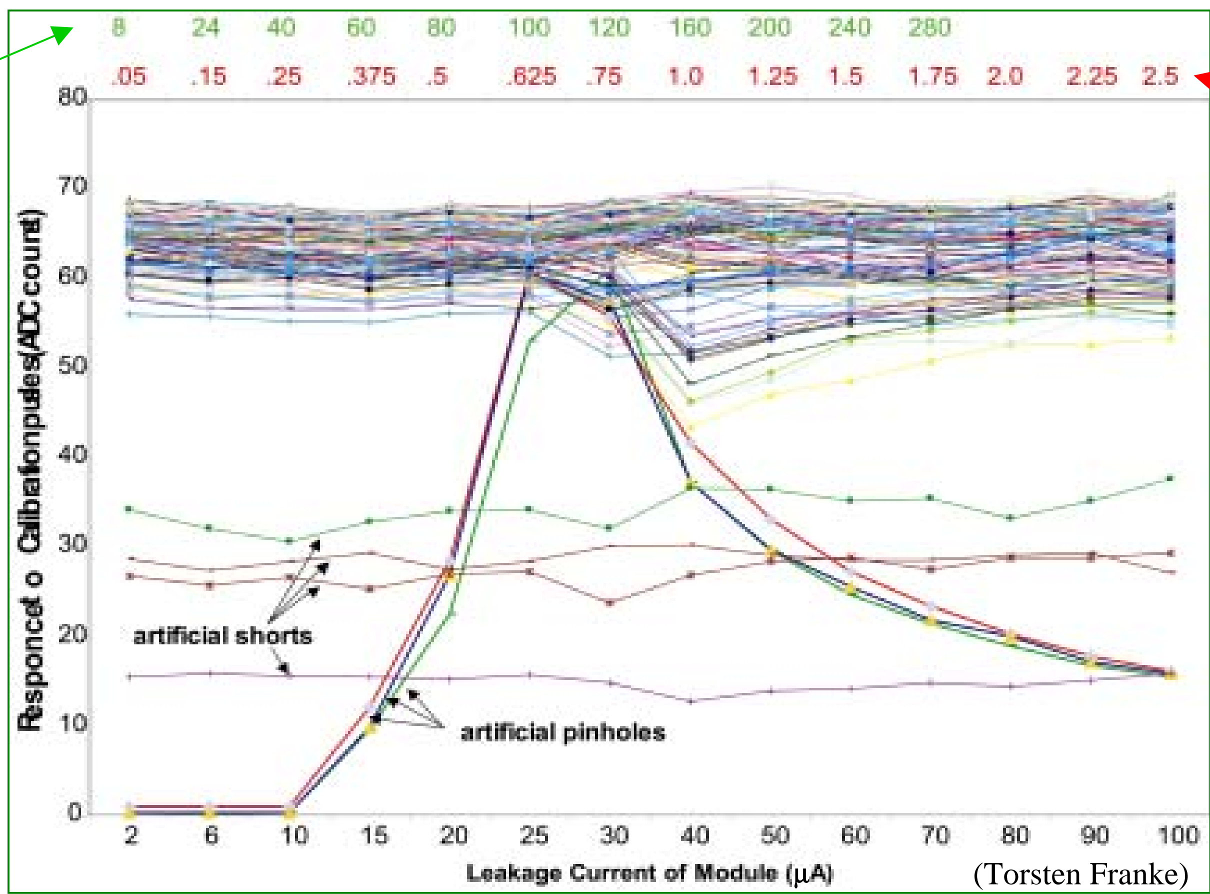


LED Pinhole Tests

Voltage conversion assumes old resistor values in bias return circuit (22KΩ,100Ω)

New Leakage Current (μA) Necessary With New Resistor Values

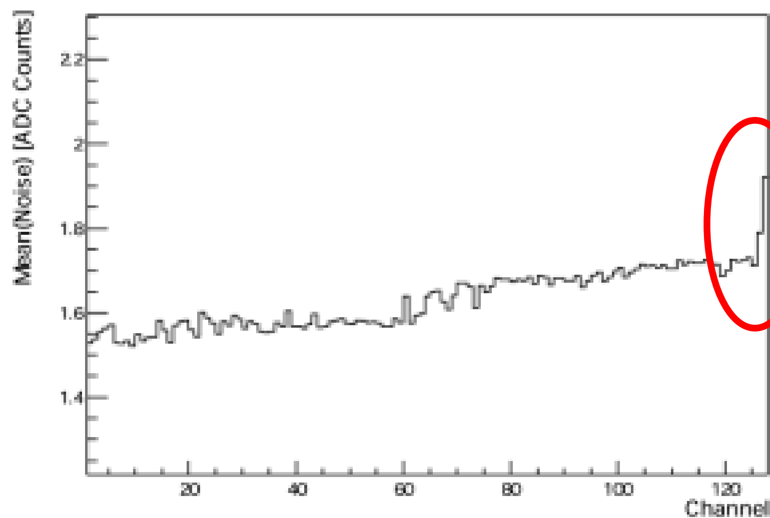
Bias Ring Voltage

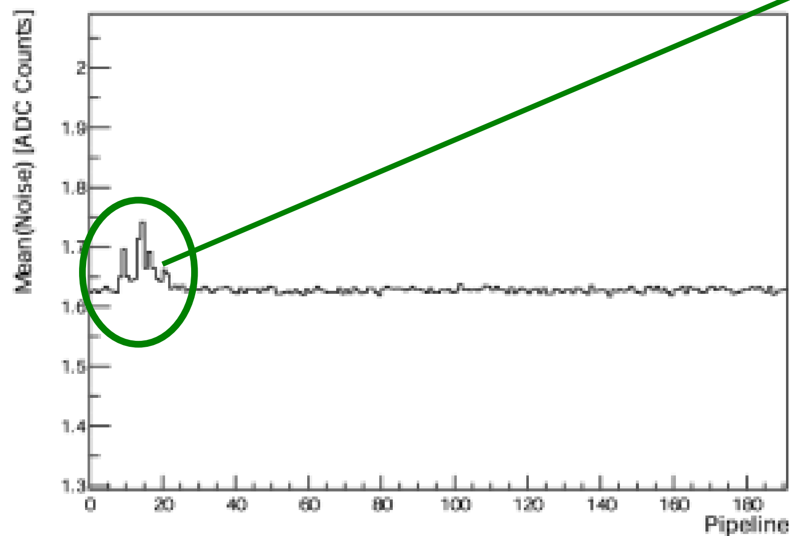


With new resistor values (2.2KΩ, 681Ω): need ~120 μA for regular pinholes
need >300 μA for "high current" pinholes

May cause damage to sensors!!!

Noise Chip Edge Wings





Increase in noise at chip edges

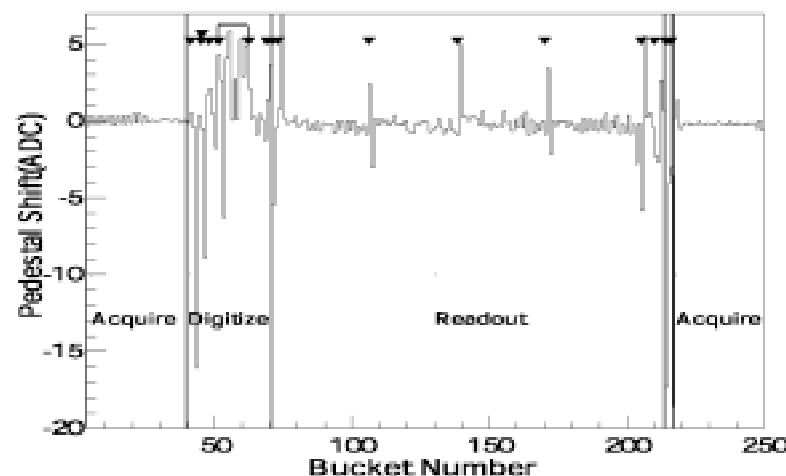
- But only in a few pipeline cells
- pipeline scan=latency scan

In-time interference effect!!

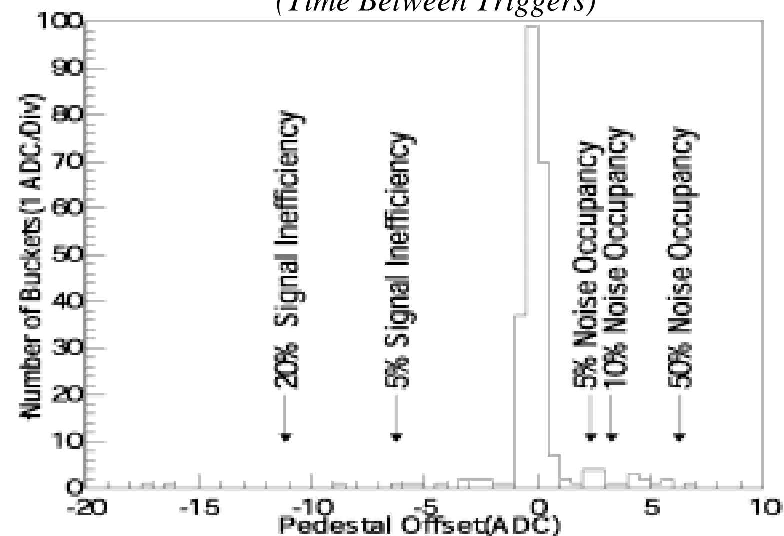
- Fairly easy to reduce/avoid
- Completely avoidable during test process

Deadtimeless Scan (ISL)

- Issue two triggers with varying time separation
  - Measure pedestal and noise at each unit of trigger separation
- With ISL, every command, chip change of state, and data readout caused pedestal shifts
  - Would guess similar effect causing wing
- Removed with DPS at CDF
- We are willing to pursue such studies



(Time Between Triggers)



Suggestions for Improved Test Model

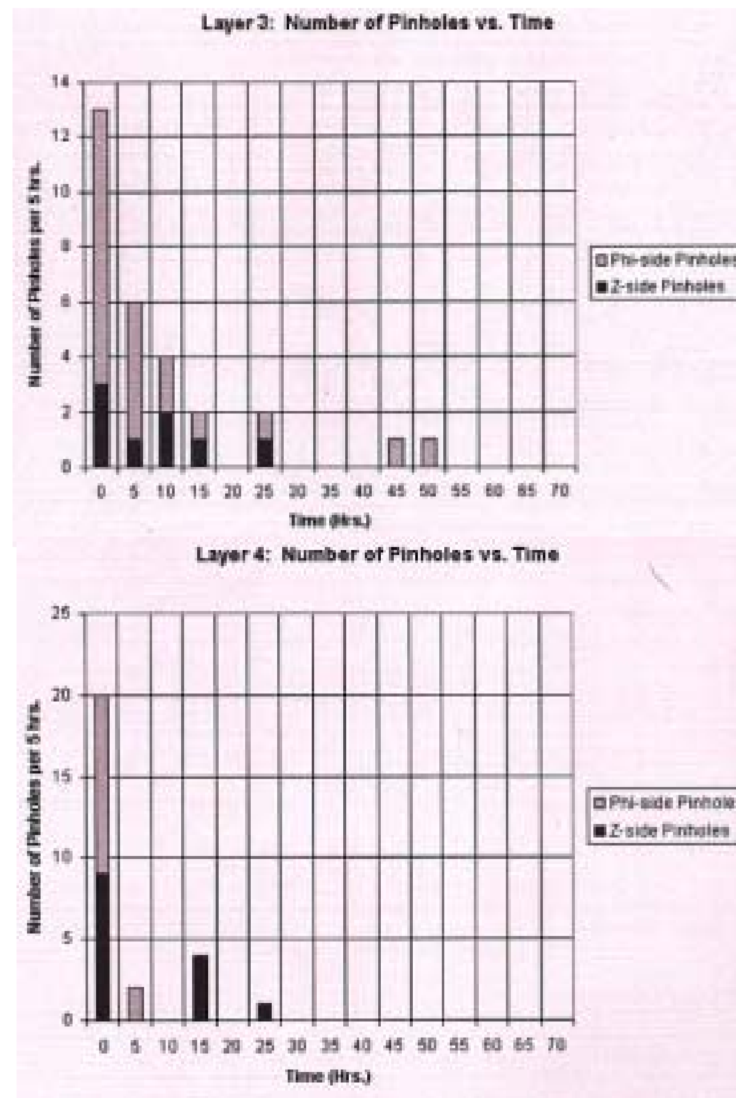
- Add to the hybrid qualification prior to pitch adaptor bonding
  - Increase understanding of hybrids by adding more pipeline and gain measurements
- Make requirements/calculation algorithms consistent through testing process
  - APV Wafer Probing→ FHIT→Strasburg →Pitch Adaptor Bonding →Module Construction→ Rod Construction/burn-in
    - Allows for the reproduction of bad channel lists
    - Eases tracking of fault creation
- Motivate requirements for fault finding and on silicon tracker performance
  - Noise Occupancy
  - Signal Efficiency
  - Signal Resolution

Suggestions for Improved Test Model(2)

- Improve system's noise performance in order to use the noise as powerful tool
  - Identification of location of opens w/o LED test
- Modify deep tests
  - Suggest different bad channel cuts specific to component type tested
  - Add fixed requirement to all percentage requirements (relative to average)
- Use cooling box as module burn-in until shown unnecessary
  - Reduces reworking during rod assembly
  - Adds important information about necessity of LED tests for the finding of some pinholes and opens locations
  - Demonstrates if hybrid burn-in necessary

CDF Module Burn-in Experience

- Significant number of pinholes created during burn-in (even after 5 hours running)
  - L1- 0.166% of strips
  - L3- 0.052% of strips
  - L4- 0.033% of strips
  - ISL-0.0071% of strips
- 7 additional pinholes created during data-taking
  - L7 burnt-in at depletion voltage
    - All other burnt in with 50% over-voltage
- Early CMS module burn-in will indicate pinhole creation rate and its effect on rod rework rate



Possible Rod Burn-in Issues

- LED systems seem necessary for discovery of “high current” pinholes and location of opens
  - In current rod burn-in plan, no LED systems available
  - May indicate need for new techniques to locate “high current” pinholes and opens
    - New sensor qualification tests, backplane pulsing, lower common mode noise, etc.
- Initial module burn-in will determine if this is an issue
  - All testing tools still available

Testing Conclusions

- Slight modification of testing program would lead to more uniform and consistent fault finding between different sites/systems
  - Reduce rework performed on completed rods
- Location of opens could be identified by combination of noise and internal calibration measurements
  - Useful for rod burn-in fault finding
- Modification of HV return circuit necessitates increase of LED intensity in pinhole search
  - "High current" pinholes may be able to be found with modification of sensor qualification
- Increase in noise at chip edges likely due to in-time interference effects
  - We would be willing to study this more thoroughly
- We are willing to help in defining testing plan/devising tests

UCSB Short-term Testing Plan

- Characterize hybrid (+PA) on arrival
  - Basic functionality, gain scan, and deep test (ARC)
- Re-characterize module on completion of construction
  - Basic functionality, gain scan, deep test, and IV curves (ARC)
- Cold box test fraction of modules (DAQ)
  - Acts as ~24 hour module burn-in
    - Identifies mechanical/bond/electrical weaknesses prior to production of large number of modules
    - Reduces reworking of rod/retrofitting of modules
- Rod construction/characterization/burn-in (when parts and test setups available)

Testing personnel at UCSB

- Professors
  - Joe Incandela
  - Claudio Campagnari
  - David Stuart
- Post-docs
  - Anthony Affolder
  - Patrick Gartung (UC-Riverside)
- Graduate Students
  - Steve Levy
  - Shawn Stromburg
  - +1-2 starting this summer
- Electrical Engineering Support
  - Sam Burke
- ESE Master Student
  - Anuroop Gupta (Database/programming)
- + Assorted Undergraduates and Techs (during full production)

Current UCSB Testing Setup

- 1 ARC Controller + 1 ARC FE
- LV & HV Power Supplies
- Dry Air
- Clamshell

- Clamshell(UCSB)
  - Plastic stand-offs
    - 2 Locating Pins
  - Kapton Extension Cables(UCSB)
    - Easy connection/disconnection
  - Solid mounting of DAQ equipment

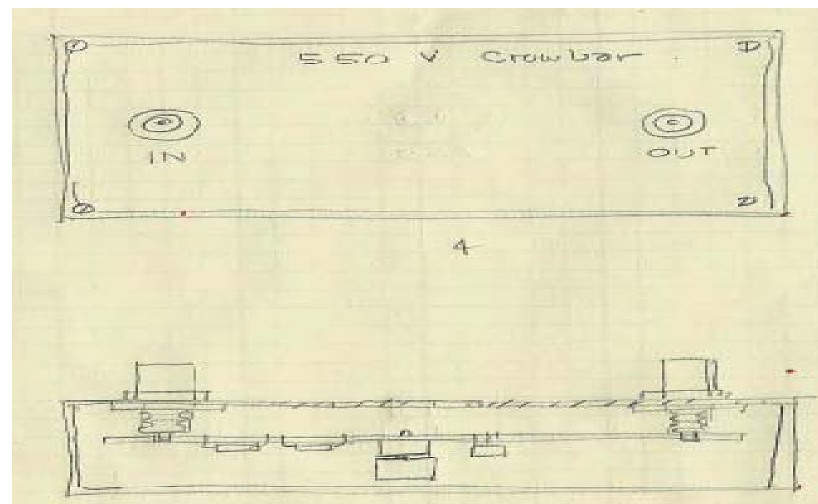
Testing Facilities

- Clean Room (5th floor Physics)
  - Adjacent to production area
  - Module tests
    - Fault finding and deep tests
  - Module burn-in station
  - Visual inspection table

- High Bay (Ground floor)
  - Rod assembly/burn-in
  - Convenient access to loading dock

Safety Protocols

- LV
  - OVP,OCP
- HV
  - Crowbar Protection
- Electrostatic Protection
  - Ground mats on tables and floors
  - Heel straps
  - Combo tester at clean room entrance
  - Touch tester at each station



(Artist Rendition)

SOS

We need full complement of test equipment

- ARC (1 of 3)
- DAQ (0 of 2)
- Vienna Cold Box
- Rod Testing Equipment
- Rod Burn-in Electronics

We're about to begin production without requisite testing equipment or experience with systems!!!!