

Module Test

Comments on Selected Topics

- Pinholes
- LV Currents
- VPSP "starting" value

Pinholes

- Pinholes already identified from sensor DB info are NOT bonded
- NEW pinholes, created during handling, bonding or thermal cycles, should be tagged by ARC or LT and then must be unbonded (then a retest could be necessary for DB)
- A few NEW pinholes have been identified during tests: are those ALL the new pinholes? We cannot be 100% sure, BUT:
- If a strip passes all tests, why we should tag it as BAD? → So that strip will be considered GOOD

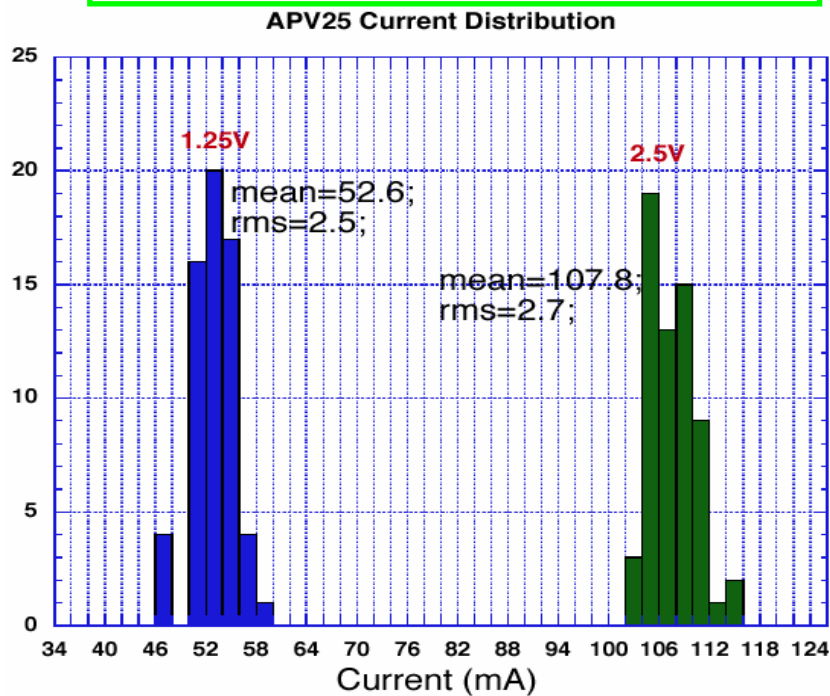
Pinholes in Sensor DB

- Going back to sensor DB: if a strip has a very low IDIEL but is classified as pinhole, and it is anyway bonded, it will probably pass all module test cuts
- If the number of such "weird" pinholes is small, we do not care
- If this number increases then there is a problem: should thresholds be changed? Are those pinholes "real" ones?
- If we create these "weird" pinholes we will not detect them, but the module will probably work satisfactorily
- Last but not least: during the pinhole test we have bulk current of hundreds of microamperes at 20 °C... and all the neighbouring APV channels works fine

LV Currents

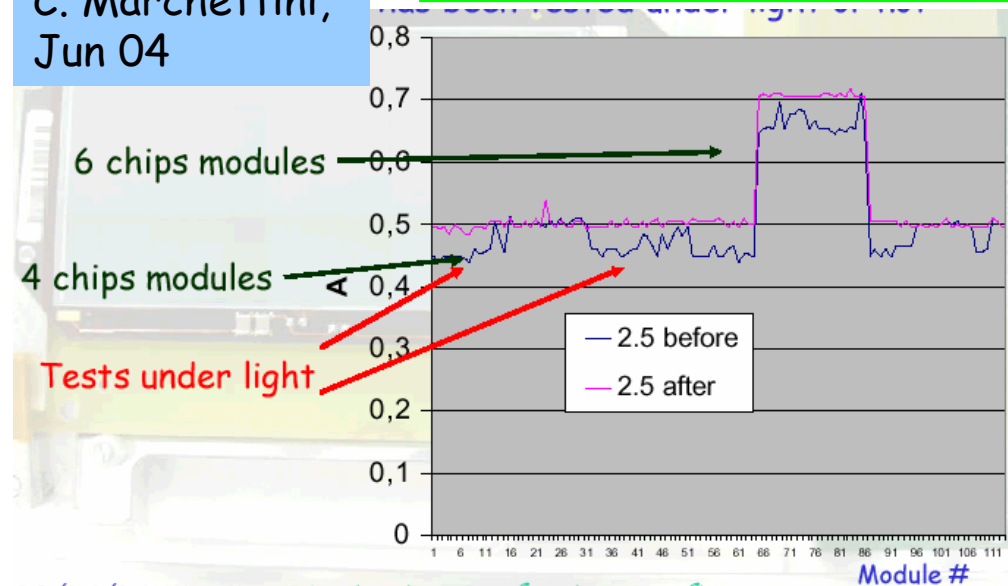
- LV investigations done in the last month:

on APV chips from I.C. data
(Nicola Bacchetta)



on TIB modules (plots & spreadsheets from all centres)

C. Marchettini,
Jun 04



LV Results in TIB from ARC Fast Test Log

PADOVA	I25 (A)	I125 (A)	
4-AVG	0.502	0.225	
STDEV	0.006	0.005	
6-AVG	0.709	0.326	Measured St Dev is generally low but average central value is different from lab to lab
STDEV	0.006	0.006	
BARI	I25	I125	Proposal:
4-AVG	0.525	0.230	•set different thresholds in ARC Fast Test for 4 and 6 APVs
STDEV	0.009	0.006	•Modules exceeding cuts must be sent to repair centres for investigations: this should help in finding possible new hybrid problems
6-AVG	0.735	0.335	
STDEV	0.011	0.008	

Possible Cuts Proposal

6 APV modules

- $I_{250} < 0.780 \text{ A}$
- $I_{125} < 0.370 \text{ A}$

4 APV modules

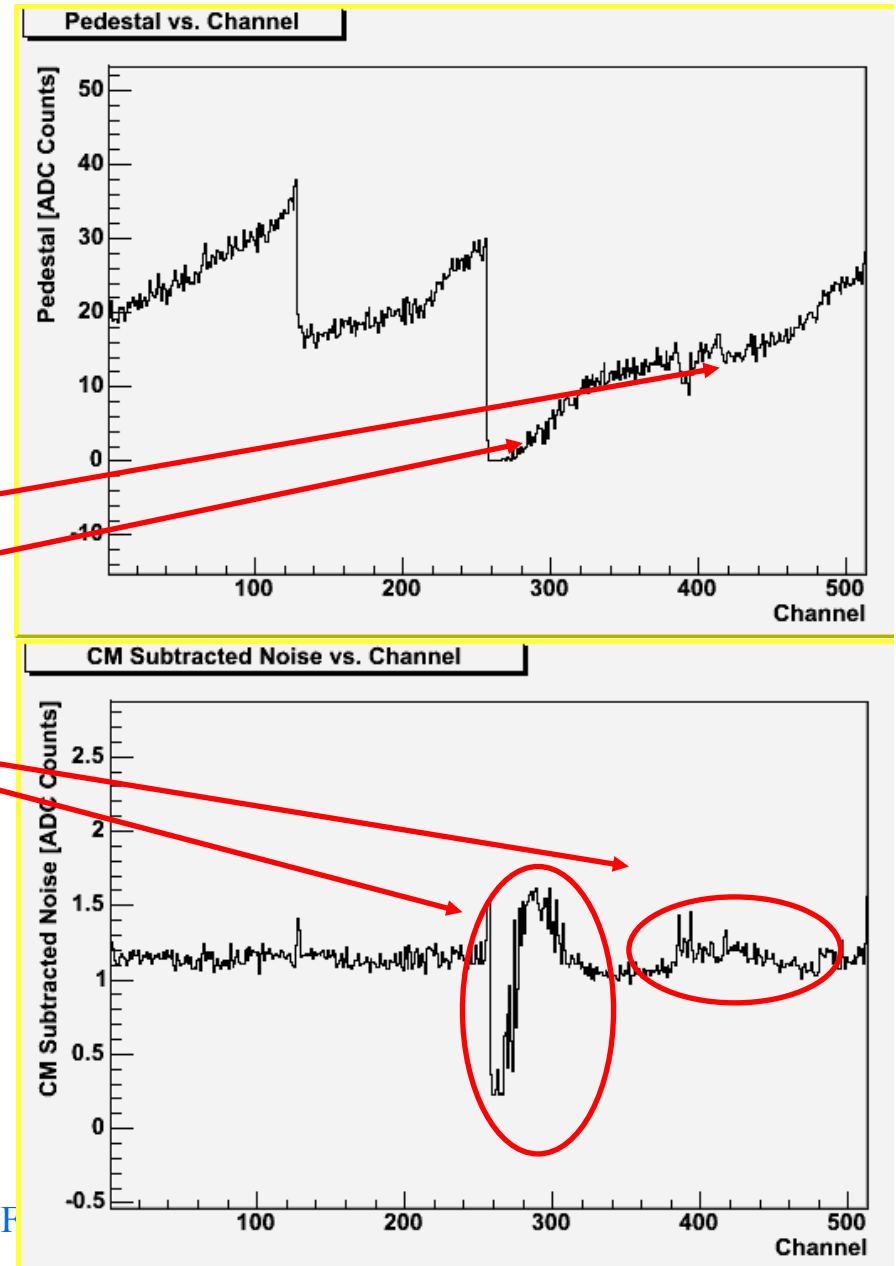
- $I_{250} < 0.550 \text{ A}$
- $I_{125} < 0.260 \text{ A}$

Those values should hold for all module types

I wait for comments on this proposal

VPSP "starting" value

- APV baseline is controlled by the register VPSP
- Pretty large variations of pedestals from chip to chip
- Low pedestals (below 20 ADC cnts in ARC) have been shown to cause bad noise figures
- Historical VPSP=40 "starting" value is not always the good one



New VPSP

- Following US and (part of) TIB experience **VPSP=35** seems a bit safer for “no stop” production, **so set it as starting value in ARC.**
- Different values are anyway possible in case of needs, under the responsibility of the local L3 manager
- **Remember!** In LT VPSP must be changed according to the different test! (Inverter ON or OFF)