US Module Testing Update

Anthony Affolder
For the US CMS tracker group

Bias Currents
Hybrid Testing Results
Arcs Testing Results
LT Testing Results and Issues

Bias Current Investigations

As requested by Marco, the US group has reviewed bias current testing requirements

- Currently modules are Grade F if bias current at 450 V exceeds 20μA
  - 5 modules out of 1973 HPK modules fail this requirement
- In June, Marco proposed removing $5xI_{expected}$ requirement
  - In US, we have not been applying this requirement
- In addition, Marco proposed if the bias current >3μA, the module should be marked as grade F until reviewed by local L3 manager
  - With 2 sensor modules, we assume that a >6μA requirement would be applied

US ST Production Modules

Bias Current (nA)

10^4, 10^3, 10^2, 10

0 50 100 150 200 250 300 350 400 450

Bias Voltage

All 98 ST modules would pass either requirement

US HPK Production Modules

Bias Current (nA)

10^4

10^3

10^2

6μA Limit

3μA Limit

0 50 100 150 200 250 300 350 400 450

Bias Voltage

L3 Intervention Requirement

Of the 1973 HPK modules, the following would fail the proposed requirements

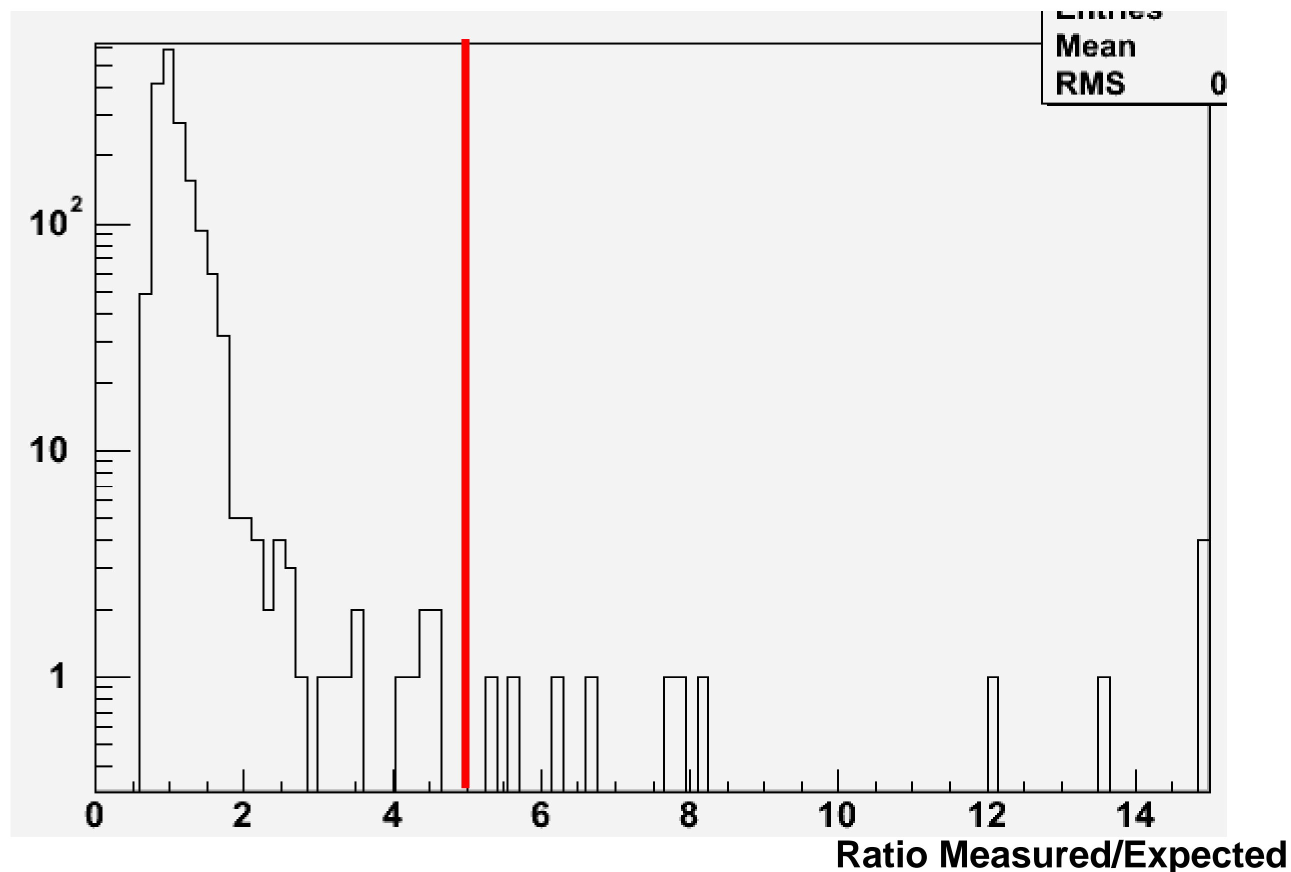
	FNAL	UCSB	Total
>3 μA	5	10	15
>6 μA	2	5	7

Most of the modules that would require intervention either had a pulled pinhole or a noisy channel

1.3% or 0.6% of the modules would require L3 intervention for the two proposed requirements

- 1 every 2.5 or 5 days at peak rate per site

$5xI_{expected}$ Requirement



13 modules would fail this requirement, 5 of which already fail the >20mA requirement

- These modules all have a noisy channel or a pulled pinhole
- This requirement fails good modules

US Conclusions

No surprises seen in either ST or HPK modules

Requiring L3 intervention on modules with >6 μA bias current is a good idea and will not be a burden

The 5x requirement does not find any truly bad modules and fails good ones

- We agree with Marco that this requirement should not be applied

Hybrid Testing Results

17 of the failures are entire chips with problems in the cold

- These are not understood and difficult to diagnose
- ***Merits further study***

13 of the failures are due to scratches in the PA which should be repairable

Rest of problems are rare chip or wire bonding failures

	Pass	Fail	% Pass
L12su	0	0	0.00%
L12sd	0	0	0.00%
L12pd	0	0	0.00%
L34p+L12pu	665	16	97.65%
L56p	1401	17	98.80%
R2N	12	0	100.00%
R2S	19	0	100.00%
R5N	111	1	99.11%
R5S	152	3	98.06%
R6	165	4	97.63%
R7	89	1	0.00%
Total	2614	42	98.42%

ARCS Testing Results

ARCS testing is proceeding very smoothly at both sites, thanks to great work of the Aachen group

- Using ARCS 8.0

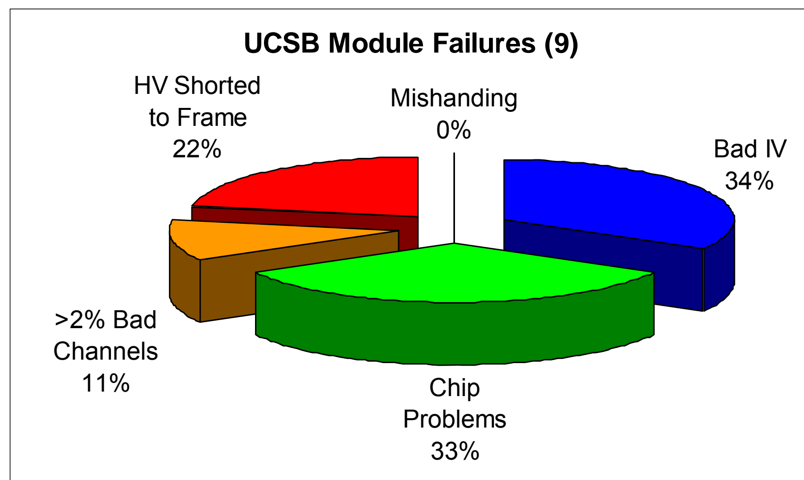
Tests take ~20 minutes and is completely automated

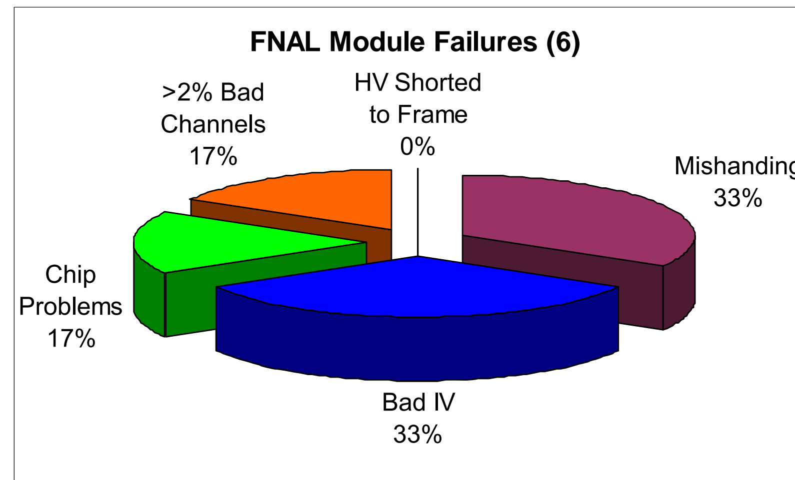
- 1 technician can run 2 stands simultaneously

Data handling fully automated with automatic uploading of xml files

	A	B	F	% A or B
L12pu	0	0	0	0.00%
L12pd	0	0	0	0.00%
L12su	0	0	0	0.00%
L12sd	0	0	0	0.00%
L34p	457	3	6	98.71%
L56p	1222	3	8	99.35%
R5N	64	1	1	98.48%
R5S	42	0	0	100.00%
R6	118	0	0	100.00%
R7	48	0	0	0.00%
Total	1951	7	15	99.24%

Module Failure Sources





Chip Problems-1 DCU address error (repairable), 2 calibration failures missed in chip testing, 1 calibration failure that developed after bonding

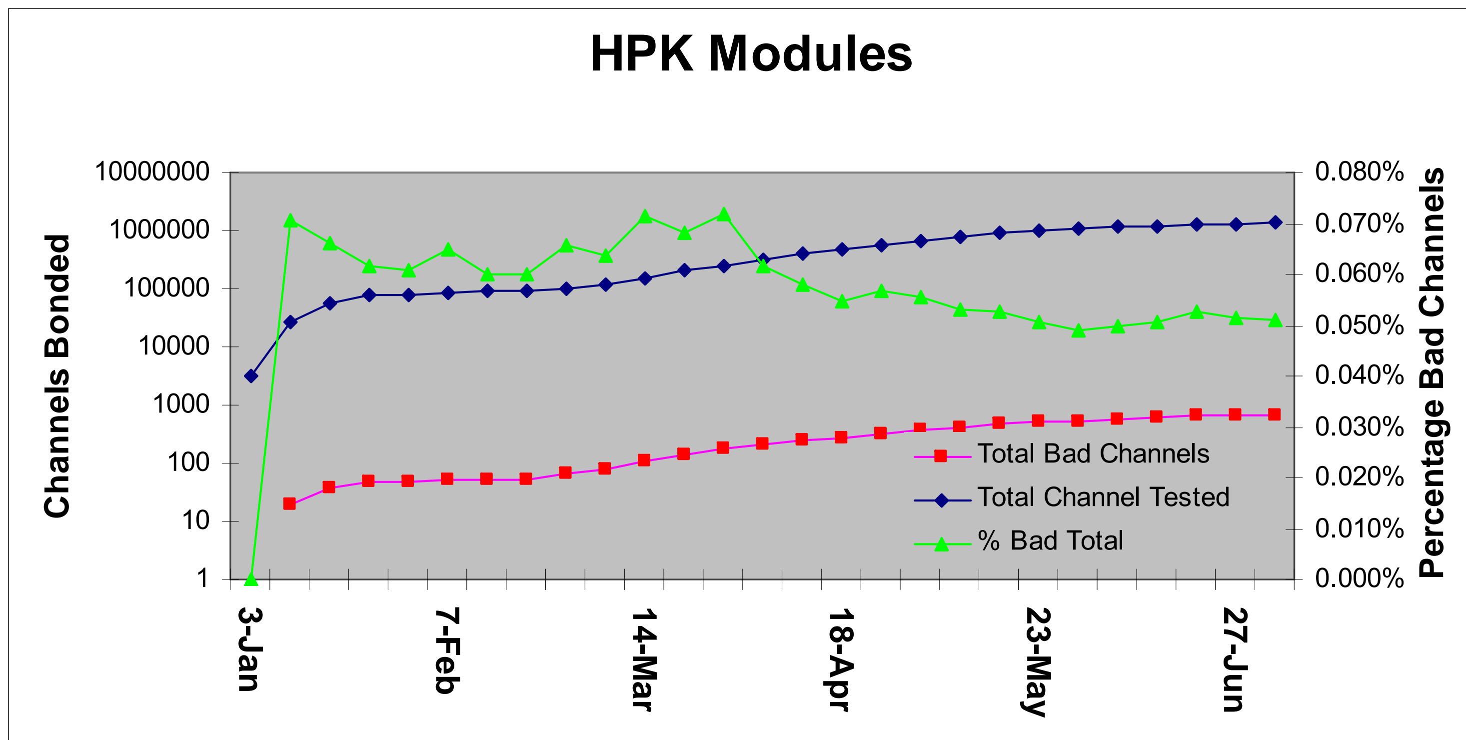
Bad IV-All 5 show damage to sensor-not clear when it occurred

HV Shorted to Frame-Should be repairable

>2% Bad Channels-Both due to wire bonding errors

Mishandling-Both occurred early in production

Module Quality



A total of 683 bad channels in the 1339128 bonded (0.051%)

- Rate of bad channels decreasing with time

Since sensors are not fully tested it is not possible to determine when the bad channels were created

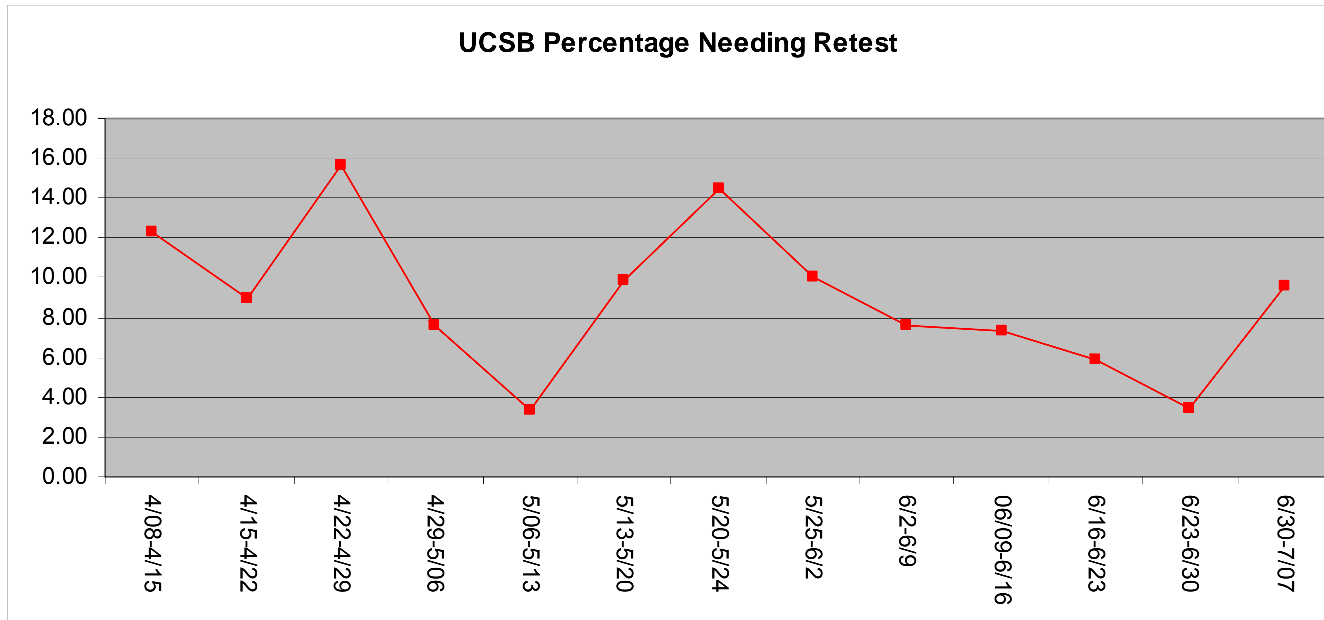
LT Testing Results

All modules have been LT tested with the data quality confirmed for each load

- Constant struggle to keep up with production
  - Only a 8-9 hour cycle possible
- UCSB is struggling against a number of failures that cause single modules to fail
- FNAL is struggling against FEC I2C and MUX errors that cause the entire load to fail and have to be re-tested
  - This will not be possible towards the end of production

	Pass	Fail	% Pass
L12pu	0	0	0.00%
L12pd	0	0	0.00%
L12su	0	0	0.00%
L12sd	0	0	0.00%
L34p	459	2	99.57%
L56p	1230	1	99.92%
R5N	68	0	100.00%
R5S	41	0	0.00%
R6	120	0	100.00%
R7	36	0	100.00%
Total	1954	3	99.85%

UCSB LT Testing Issues

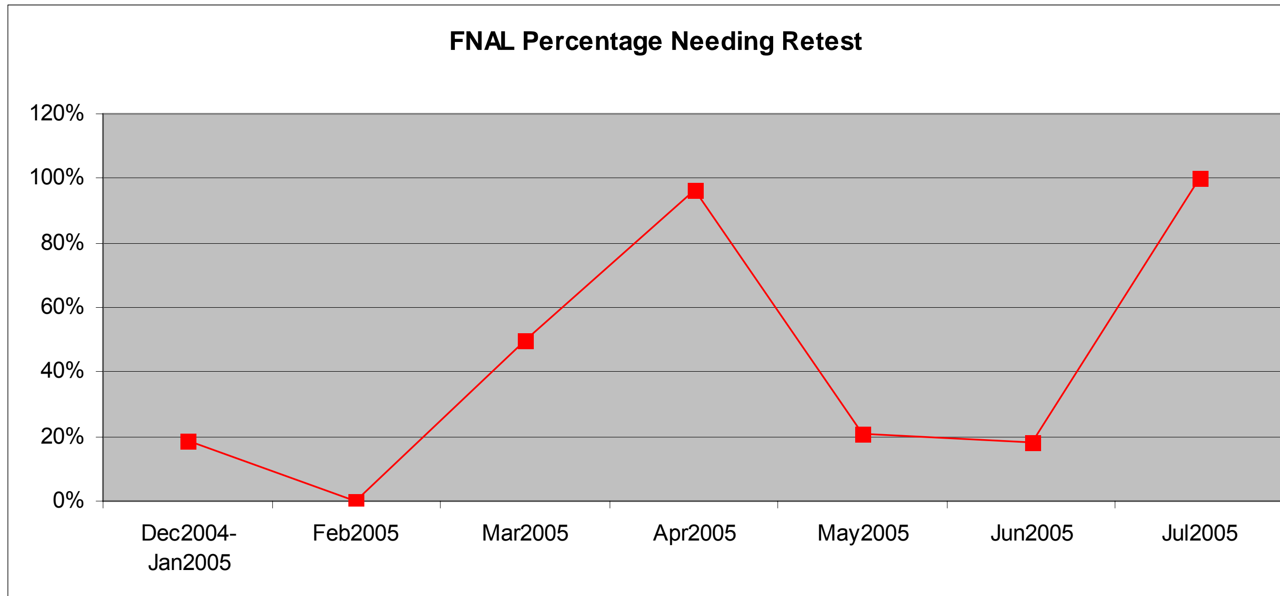


By adding slot extenders and through constant monitoring the rate of re-testing has reduced to 5-8%

- Problems now appear to be irreducible

Dominant causes of test failure are lack of xml generation, new bad channels in cold, single slot CMN noise, and resistive pin contact

FNAL LT Testing Issues



Constant global failures of modules require almost constant operation of cold box

- Will not be possible at higher production rates

In March and April, FEC I2C errors were dominant cause of failures

- Replacing CCUs removed errors

Since May, MUX I2C errors have become the dominant problem

MUX Problems

KAR-MUX errors

- Message in log file KAR-MUX i2c error
- Then:
  - Software exits
  - Software exits with a Break segmentation fault message
  - Scenario keeps running, but the data for the record/test when the error occurred looks bad

DAQ errors (MUX Trips)

- Message in logfile-flush function failed after XXX retries, restart daq
- At the same time, FED server keeps reloading Xilinx
- And at the same time one can hear the MUX clicking
  - A channel trip state
- Result-empty histograms for noise, ped, cal pulses

It is not clear if these are caused by the software, the TSC, the TPO, or the MUX system. Any help would be greatly appreciated.

Conclusions

High quality hybrids and modules are being produced

- 98.4% of hybrids pass cold testing
  - But chip failures in cold needs further study
- 99.2% of modules pass ARCS testing
  - 0.05% bad channels
- 99.85% of modules pass LT testing

Hybrid and module testing keeping up with production

- But high rate of LT test failures could be potential bottleneck
- *We need to solve MUX problems at FNAL or production could be effected*