



**C M S**  
Compact Muon Solenoid

***Testing  
Hybrids with Pitch Adapter  
and  
TOB Module #11  
using ARC system***

---

CERN hybrid &  
module test station

Module Test Meeting  
05.03.2002

Michael Pöttgens, Giacomo Sguazzoni



# Test Objects

---

- 15 hybrids tested

(302166302000x;x={07,12,13,17,20,22,23,25,26,27,29,48,56})

-> are used at CERN for rod test and DAQ setups

- 13 hybrids with pitch adapter tested

(302166302000x;x={06,39,41,43,46,47,48,49,50,52,54,55,56,57,59})

-> 11 sent to Lyon for tec expressline

-> 2 sent to Vienna for tec expressline

-> purpose of test station

- tob module #11

(hybrid 30216630200016, frame 11)

-> to be send to Torino



## *Measurements done*

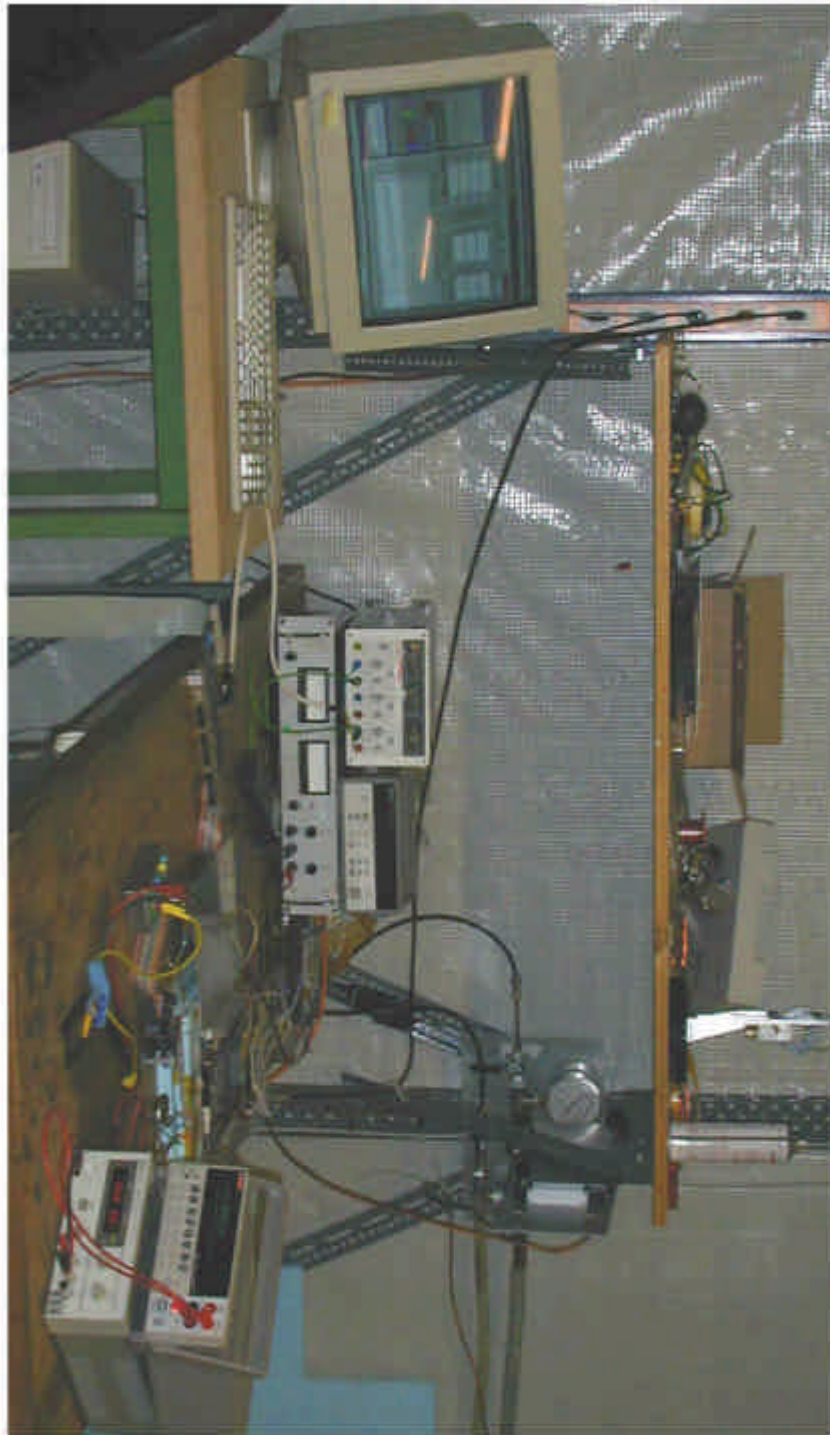
---

- take pedestals & noise
  - > at least 10kevents per piece
  
- pulse shapes
  - > just for some hybrids
    - storing pulse shape data was not a feature of ARCS at that time (now it is, version ARCS 4.0 beta)
  
- thermal cycling test
  - > one Hybrid with pitch adapter and module #11



# *test setup*

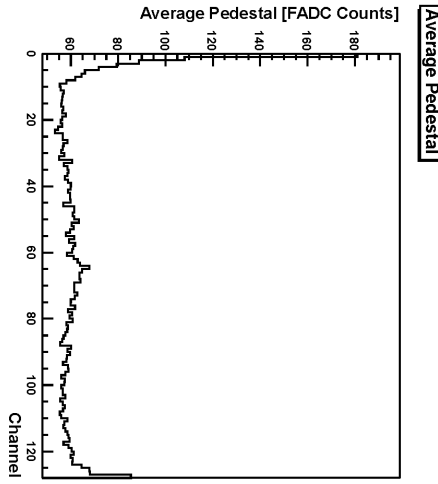
---





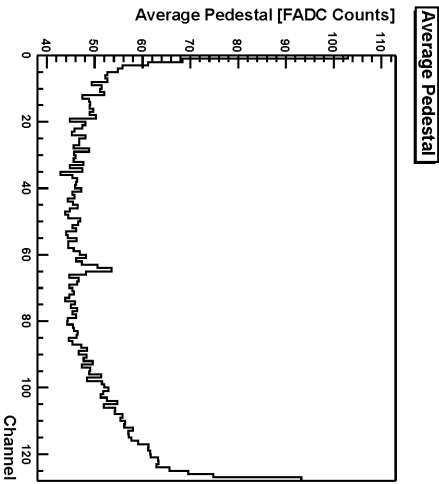
# Hybrid #22 Pedestals

Chip Settings:  
 DCC.Address=64  
 Mode=11  
 Latency=4  
 DPRE=98  
 DPCASC=52  
 DSP=34  
 ISHA=34  
 ISSR=34  
 DSP=55  
 DMCXIN=34  
 ISHARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSRP=40  
 CDRV=254  
 CSBL=1  
 MEXGAN=4  
 Error=0  
 MIX\_Res=3  
 P.L1\_1=1  
 P.L1\_2=0  
 P.L1\_3=127  
 P.L1\_4=0  
 P.L1\_5=0



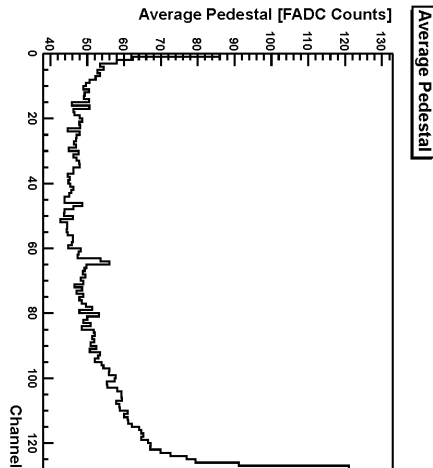
0x40

Chip Settings:  
 DCC.Address=72  
 Mode=11  
 Latency=4  
 DPRE=98  
 DPCASC=52  
 DSP=34  
 ISHA=34  
 ISSR=34  
 DSP=55  
 DMCXIN=34  
 ISHARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSRP=40  
 CDRV=254  
 CSBL=1  
 MEXGAN=4  
 Error=0  
 MIX\_Res=3  
 P.L1\_1=1  
 P.L1\_2=0  
 P.L1\_3=127  
 P.L1\_4=0  
 P.L1\_5=0



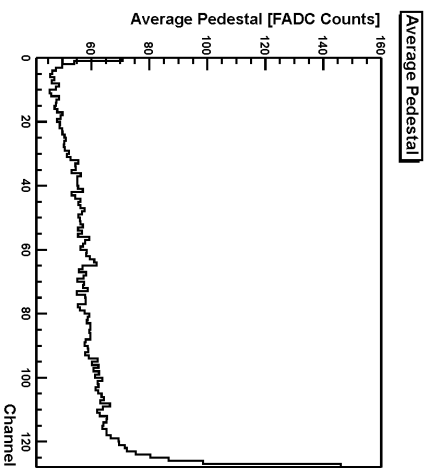
0x48

Chip Settings:  
 DCC.Address=66  
 Mode=11  
 Latency=4  
 DPRE=98  
 DPCASC=52  
 DSP=34  
 ISHA=34  
 ISSR=34  
 DSP=55  
 DMCXIN=34  
 ISHARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSRP=40  
 CDRV=254  
 CSBL=1  
 MEXGAN=4  
 Error=0  
 MIX\_Res=3  
 P.L1\_1=1  
 P.L1\_2=0  
 P.L1\_3=127  
 P.L1\_4=0  
 P.L1\_5=0



0x42

Chip Settings:  
 DCC.Address=74  
 Mode=11  
 Latency=4  
 DPRE=98  
 DPCASC=52  
 DSP=34  
 ISHA=34  
 ISSR=34  
 DSP=55  
 DMCXIN=34  
 ISHARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSRP=40  
 CDRV=254  
 CSBL=1  
 MEXGAN=4  
 Error=0  
 MIX\_Res=3  
 P.L1\_1=1  
 P.L1\_2=0  
 P.L1\_3=127  
 P.L1\_4=0  
 P.L1\_5=0

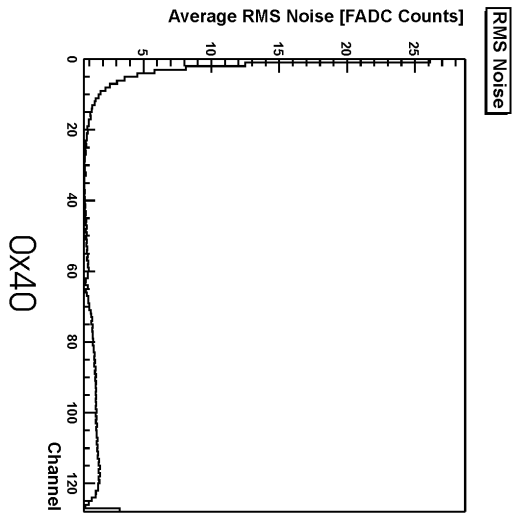


0x4c

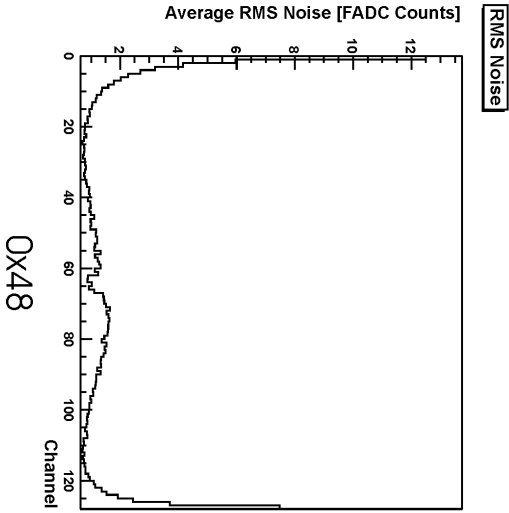


# Hybrid #22 Noise

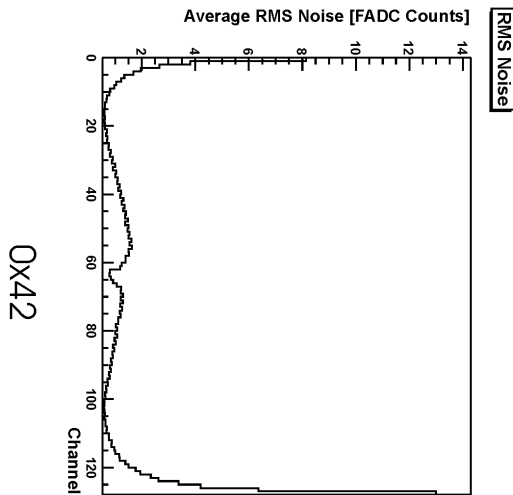
Chip Settings:  
 I2C\_Address=64  
 Mode=11  
 Latency=4  
 IPRR=98  
 IPCASC=52  
 IPR=34  
 ISHA=34  
 ISSP=34  
 IPRP=55  
 IMUXIN=34  
 ISPARB=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSP=40  
 CDRV=254  
 CSRL=1  
 MUXGAN=4  
 Error=0  
 MUX\_Ke=3  
 PTL\_1=1  
 PTL\_2=0  
 PTL\_3=127  
 PTL\_4=0  
 PTL\_5=0



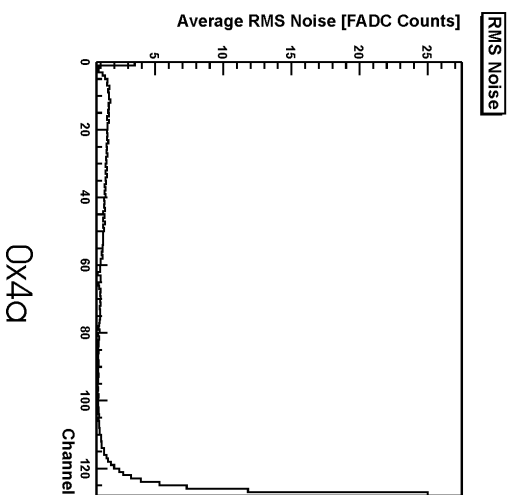
Chip Settings:  
 I2C\_Address=72  
 Mode=11  
 Latency=4  
 IPRR=98  
 IPCASC=52  
 IPR=34  
 ISHA=34  
 ISSP=34  
 IPRP=55  
 IMUXIN=34  
 ISPARB=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSP=40  
 CDRV=254  
 CSRL=1  
 MUXGAN=4  
 Error=0  
 MUX\_Ke=3  
 PTL\_1=1  
 PTL\_2=0  
 PTL\_3=127  
 PTL\_4=0  
 PTL\_5=0



Chip Settings:  
 I2C\_Address=66  
 Mode=11  
 Latency=4  
 IPRR=98  
 IPCASC=52  
 IPR=34  
 ISHA=34  
 ISSP=34  
 IPRP=55  
 IMUXIN=34  
 ISPARB=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSP=40  
 CDRV=254  
 CSRL=1  
 MUXGAN=4  
 Error=0  
 MUX\_Ke=3  
 PTL\_1=1  
 PTL\_2=0  
 PTL\_3=127  
 PTL\_4=0  
 PTL\_5=0



Chip Settings:  
 I2C\_Address=74  
 Mode=11  
 Latency=4  
 IPRR=98  
 IPCASC=52  
 IPR=34  
 ISHA=34  
 ISSP=34  
 IPRP=55  
 IMUXIN=34  
 ISPARB=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VSP=40  
 CDRV=254  
 CSRL=1  
 MUXGAN=4  
 Error=0  
 MUX\_Ke=3  
 PTL\_1=1  
 PTL\_2=0  
 PTL\_3=127  
 PTL\_4=0  
 PTL\_5=0

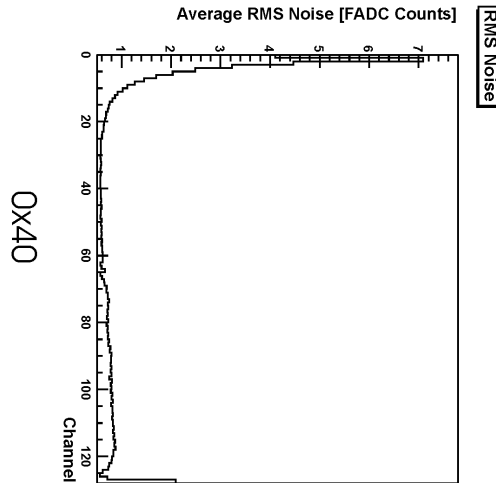




# Hybrid #20 Noise

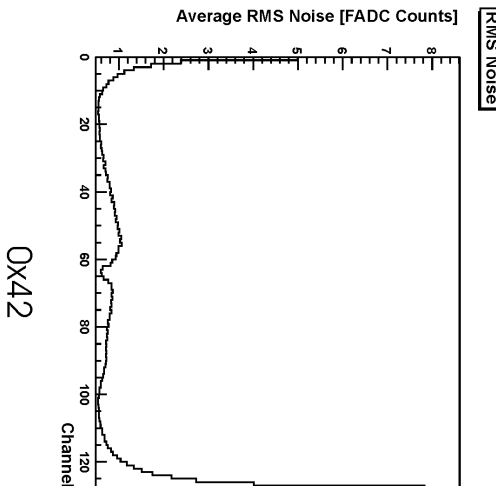
Chip Settings:  
DCC.Address=64

Mode=11
Latency=4
IPCCASC=2
IPSP=34
ISHA=34
ISSP=34
IPSP=45
IMUXIN=34
ISBARE=0
ICAL=29
VFP=30
VFS=60
VSP=40
CBRV=24
CSSEL=1
MIXGAIN=4
Error=0
MIX_Res=3
PLL_1=1
PLL_2=0
PLL_3=127
PLL_4=0
PLL_5=0



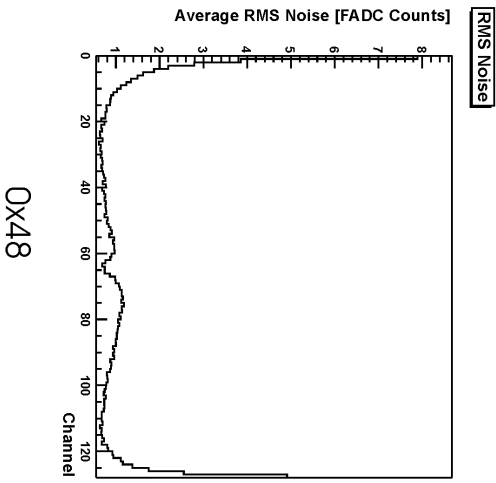
Chip Settings:  
DCC.Address=66

Mode=11
Latency=4
IPRC=98
IPCCASC=2
IPSP=34
ISHA=34
ISSP=34
IPSP=45
IMUXIN=34
ISBARE=0
ICAL=29
VFP=30
VFS=60
VSP=40
CBRV=24
CSSEL=1
MIXGAIN=4
Error=0
MIX_Res=3
PLL_1=1
PLL_2=0
PLL_3=127
PLL_4=0
PLL_5=0



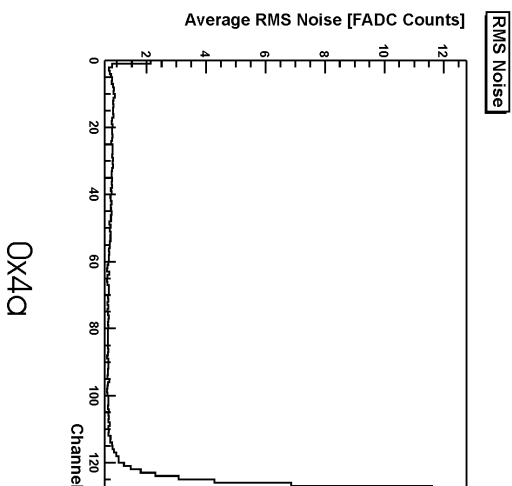
Chip Settings:  
DCC.Address=72

Mode=11
Latency=4
IPRC=98
IPCCASC=2
IPSP=34
ISHA=34
ISSP=34
IPSP=45
IMUXIN=34
ISBARE=0
ICAL=29
VFP=30
VFS=60
VSP=40
CBRV=24
CSSEL=1
MIXGAIN=4
Error=0
MIX_Res=3
PLL_1=1
PLL_2=0
PLL_3=127
PLL_4=0
PLL_5=0



Chip Settings:  
DCC.Address=74

Mode=11
Latency=4
IPRC=98
IPCCASC=2
IPSP=34
ISHA=34
ISSP=34
IPSP=45
IMUXIN=34
ISBARE=0
ICAL=29
VFP=30
VFS=60
VSP=40
CBRV=24
CSSEL=1
MIXGAIN=4
Error=0
MIX_Res=3
PLL_1=1
PLL_2=0
PLL_3=127
PLL_4=0
PLL_5=0

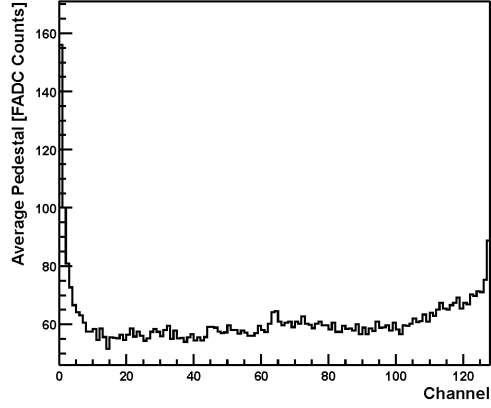




# Hybrid #27 Pedestals

Chip Settings:  
I2C.Address=64  
Mode=11  
Latency=4  
IPRE=98  
IPCASC=52  
IPSF=34  
ISHA=34  
ISSF=34  
IPSP=55  
IMUXIN=34  
ISPARE=0  
ICAL=29  
VFP=30  
VFS=60  
VPSP=40  
CDRV=254  
CSEL=1  
MUXGAIN=4  
Error=0  
MUX\_Res=3  
PLL\_1=1  
PLL\_2=0  
PLL\_3=127  
PLL\_4=0  
PLL\_5=0

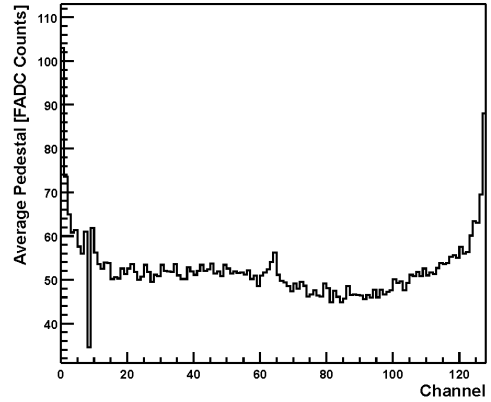
Average Pedestal



0x40

Chip Settings:  
I2C.Address=72  
Mode=11  
Latency=4  
IPRE=98  
IPCASC=52  
IPSF=34  
ISHA=34  
ISSF=34  
IPSP=55  
IMUXIN=34  
ISPARE=0  
ICAL=29  
VFP=30  
VFS=60  
VPSP=40  
CDRV=254  
CSEL=1  
MUXGAIN=4  
Error=0  
MUX\_Res=3  
PLL\_1=1  
PLL\_2=0  
PLL\_3=127  
PLL\_4=0  
PLL\_5=0

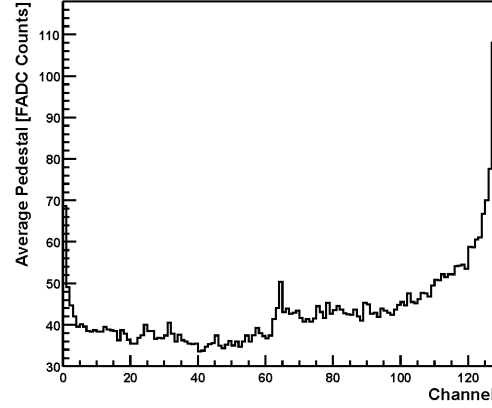
Average Pedestal



0x48

Chip Settings:  
I2C.Address=66  
Mode=11  
Latency=4  
IPRE=98  
IPCASC=52  
IPSF=34  
ISHA=34  
ISSF=34  
IPSP=55  
IMUXIN=34  
ISPARE=0  
ICAL=29  
VFP=30  
VFS=60  
VPSP=40  
CDRV=254  
CSEL=1  
MUXGAIN=4  
Error=0  
MUX\_Res=3  
PLL\_1=1  
PLL\_2=0  
PLL\_3=127  
PLL\_4=0  
PLL\_5=0

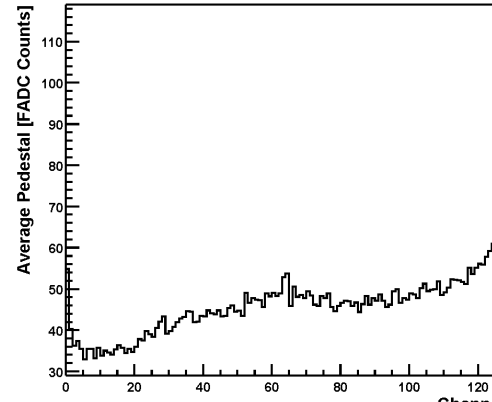
Average Pedestal



0x42

Chip Settings:  
I2C.Address=74  
Mode=11  
Latency=4  
IPRE=98  
IPCASC=52  
IPSF=34  
ISHA=34  
ISSF=34  
IPSP=55  
IMUXIN=34  
ISPARE=0  
ICAL=29  
VFP=30  
VFS=60  
VPSP=40  
CDRV=254  
CSEL=1  
MUXGAIN=4  
Error=0  
MUX\_Res=3  
PLL\_1=1  
PLL\_2=0  
PLL\_3=127  
PLL\_4=0  
PLL\_5=0

Average Pedestal

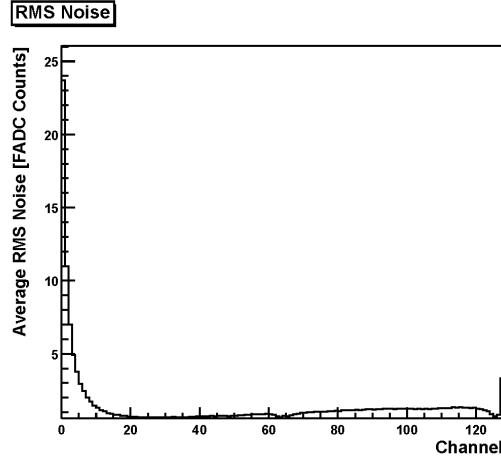


0x4a



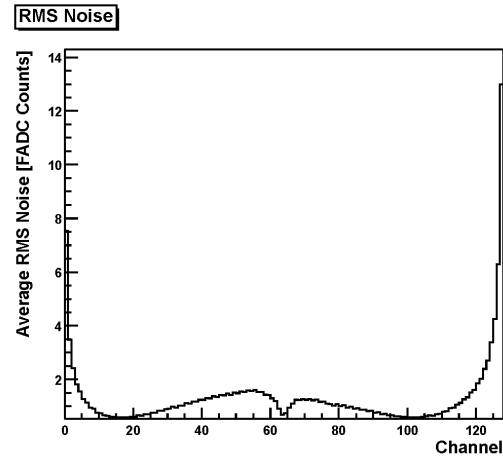
# Hybrid #27 Noise

Chip Settings:  
 I2C.Address=64  
 Mode=11  
 Latency=4  
 IPRE=98  
 IPCASC=52  
 IPSF=34  
 ISHA=34  
 ISSF=34  
 IPSP=55  
 IMUXIN=34  
 ISPARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VPSP=40  
 CDRV=254  
 CSEL=1  
 MUXGAIN=4  
 Error=0  
 MUX\_Res=3  
 PLL\_1=1  
 PLL\_2=0  
 PLL\_3=127  
 PLL\_4=0  
 PLL\_5=0



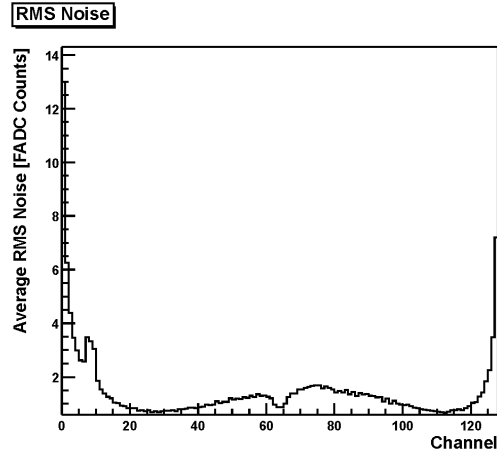
0x40

Chip Settings:  
 I2C.Address=66  
 Mode=11  
 Latency=4  
 IPRE=98  
 IPCASC=52  
 IPSF=34  
 ISHA=34  
 ISSF=34  
 IPSP=55  
 IMUXIN=34  
 ISPARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VPSP=40  
 CDRV=254  
 CSEL=1  
 MUXGAIN=4  
 Error=0  
 MUX\_Res=3  
 PLL\_1=1  
 PLL\_2=0  
 PLL\_3=127  
 PLL\_4=0  
 PLL\_5=0



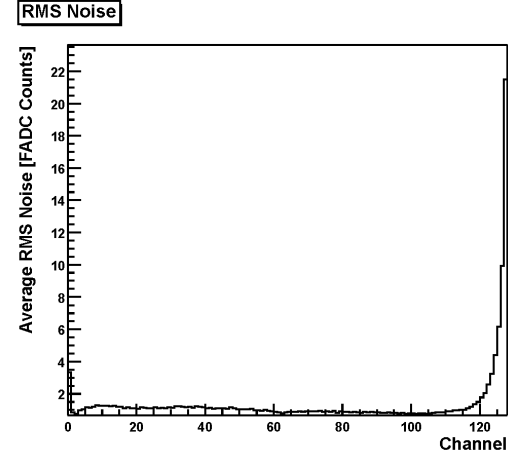
0x42

Chip Settings:  
 I2C.Address=72  
 Mode=11  
 Latency=4  
 IPRE=98  
 IPCASC=52  
 IPSF=34  
 ISHA=34  
 ISSF=34  
 IPSP=55  
 IMUXIN=34  
 ISPARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VPSP=40  
 CDRV=254  
 CSEL=1  
 MUXGAIN=4  
 Error=0  
 MUX\_Res=3  
 PLL\_1=1  
 PLL\_2=0  
 PLL\_3=127  
 PLL\_4=0  
 PLL\_5=0



0x4a

Chip Settings:  
 I2C.Address=74  
 Mode=11  
 Latency=4  
 IPRE=98  
 IPCASC=52  
 IPSF=34  
 ISHA=34  
 ISSF=34  
 IPSP=55  
 IMUXIN=34  
 ISPARE=0  
 ICAL=29  
 VFP=30  
 VFS=60  
 VPSP=40  
 CDRV=254  
 CSEL=1  
 MUXGAIN=4  
 Error=0  
 MUX\_Res=3  
 PLL\_1=1  
 PLL\_2=0  
 PLL\_3=127  
 PLL\_4=0  
 PLL\_5=0



0x4a



## Results

---

found out:

- all hybrids worked  
(problems with apv i2c communication  
after access of dcu -> talk of Makus Axer  
in hybrid test meeting)
- noise of hybrids with pitch adapter is much  
higher than noise of bare hybrid
- traceability of opens between hybrid &  
pitch adapter
- but noise is much higher than in earlier  
measurements

were does noise come from?

- ⇒ test with cms like system also showed high noise
- ⇒ is noise caused by new hybrids somehow?



## *Investigation*

---

glued pitch adapter & one of the old  
(CERN made) hybrids to carbon fiber

- noise was still as high as before  
=> not a hybrid problem
- checked grounding  
grounding was bad: signals of 3V 50Hz

new measurements showed noise  
close to hybrid level!

- ⇒ pitch adapter works like an antenna
- ⇒ traceability for defects



## *Thermal Cycling Tests*

---

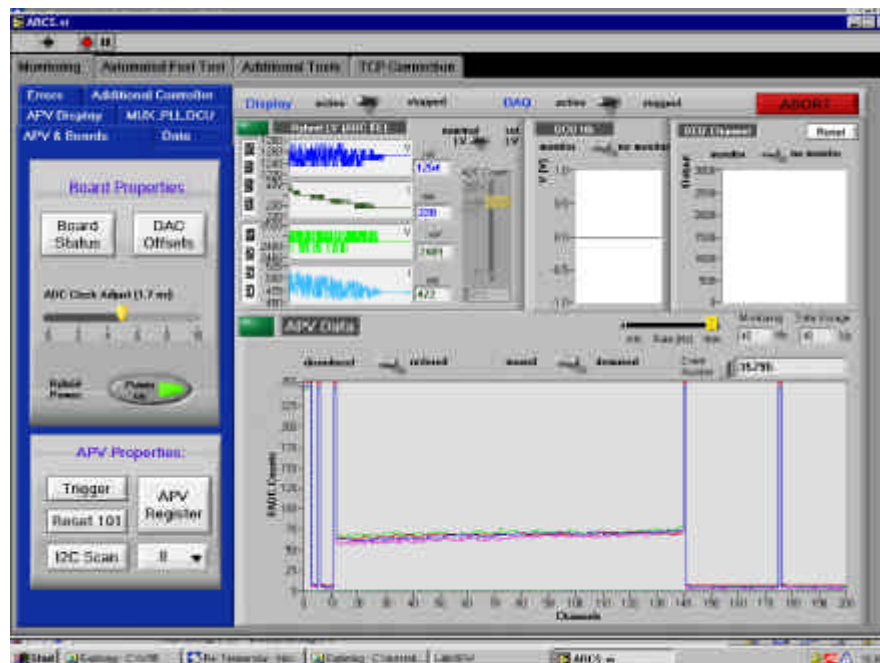
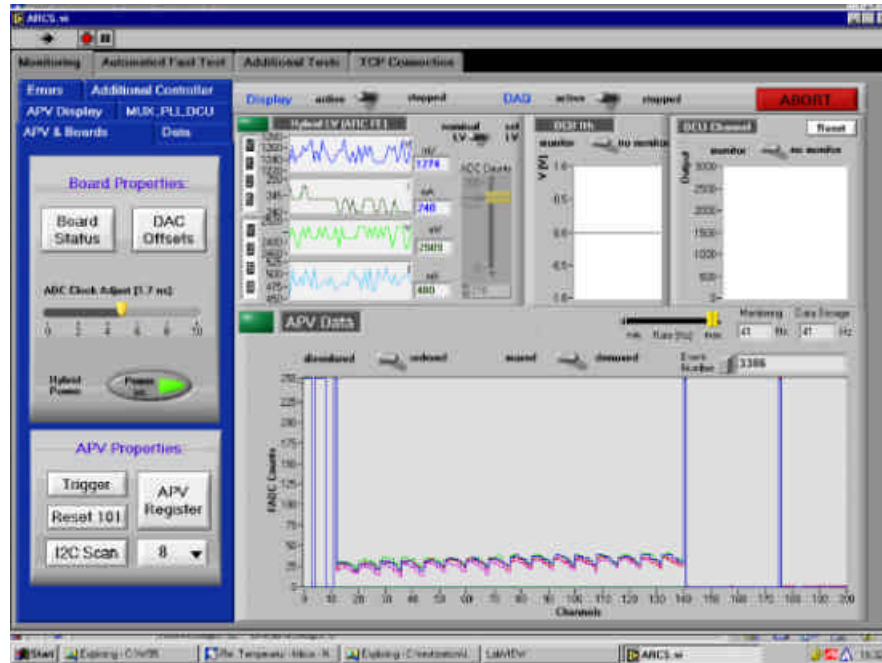
- cooling with peltier
- ARC FE Adapter inside box connected via NAIS
- power converting part of FE adapter stayed outside cool box
- monitored humidity & measured temperature via ntc resistors

observation:

- at about  $-10^{\circ}\text{C}$  baseline starts to jump up and down
- data shows a regular structure
- V125 and V250 move up and down
- noise increases



# Screenshots

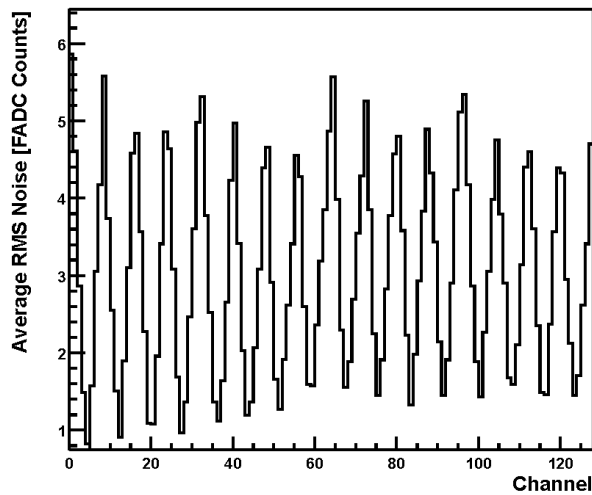


# Explanation

```

Chip Settings:
I2C.Address=64
Mode=11
Latency=4
IPRE=98
IPCASC=52
IPSF=34
ISHA=34
ISSF=34
IPSP=55
IMUXIN=34
ISPARE=0
ICAL=29
VFP=30
VFS=60
VPSP=40
CDRV=254
CSEL=1
MUXGAIN=4
Error=0
MUX_Res=3
PLL_1=1
PLL_2=0
PLL_3=127
PLL_4=0
PLL_5=0
    
```

RMS Noise



- capacitance of capacitors is reduced with decreasing temperature  
=> voltage is not constant

=> current version of FE adapter  
can **not** be used in cold  
environment!

## *Solution*

---



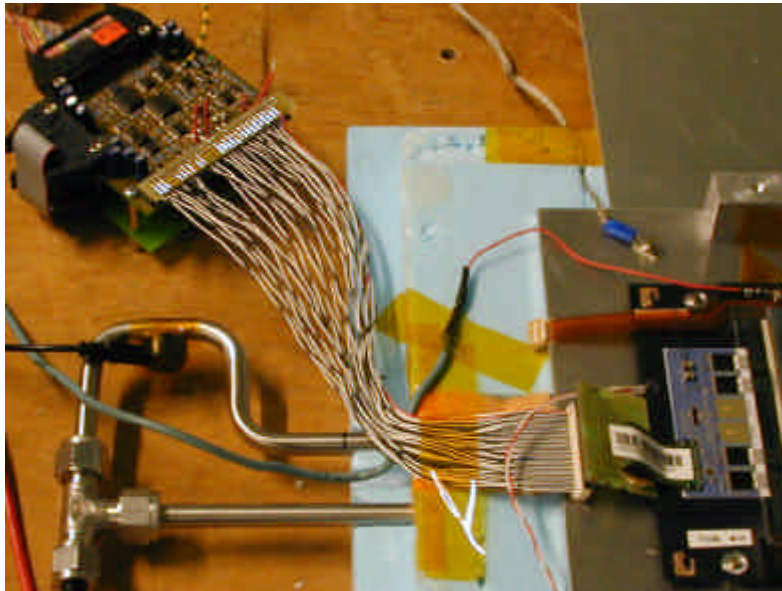
mounting of **tantal** capacitors  
solves problem!

⇒ exchange capacitors if adapter  
is supposed to be used in cold  
environment

## *Adaption of Test Setup*

---

connection FE adapter - test object via  
SAMTEC/ERNIE adaptercable + small  
adaptercard ERNIE/NAIS



⇒ adapter stays outside test box

but

⇒ bad influence on signal performance

⇒ shielding of cable necessary?



# *Test of Hybrid with Pitch Adapter glued to Carbon Fiber @-30°C*

- cooling down to  $-30^{\circ}\text{C}$  in 15min
- using adapter cable & small adapter card
- relative humidity less than 20%
- taking pedestal & noise data

test was successful:

- no failing bonds
- no problems with apv data
- dcu showed identical data on all channel(changed at  $-25^{\circ}\text{C}$ )

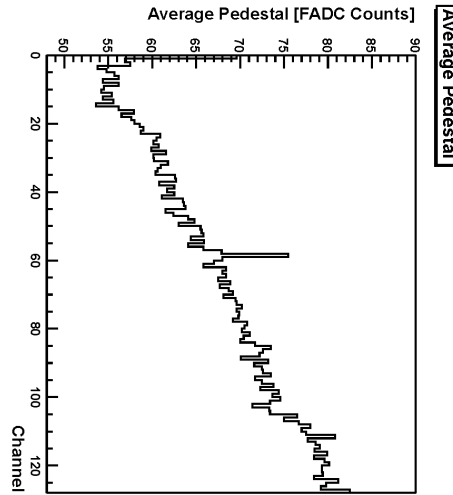
=> prepared for module thermal cycling



# Module #11 Pedestals @ 20°C

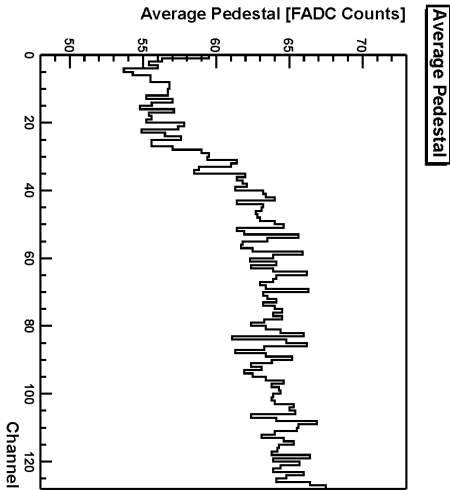
```

Chip Settings:
DC-Address= 64
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VFS= 60
VSR= 40
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L. 1= 1
P.L. 2= 0
P.L. 3= 127
P.L. 4= 0
P.L. 5= 0
  
```



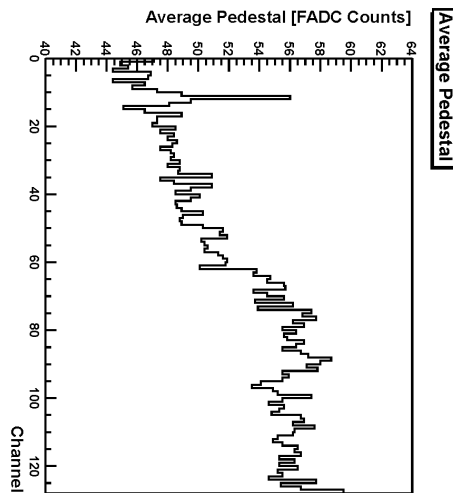
```

Chip Settings:
DC-Address= 72
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VFS= 60
VSR= 40
CDR= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L. 1= 1
P.L. 2= 0
P.L. 3= 127
P.L. 4= 0
P.L. 5= 0
  
```



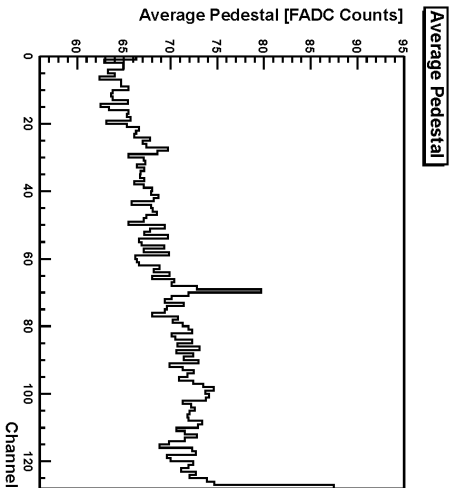
```

Chip Settings:
DC-Address= 66
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VFS= 60
VSR= 40
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L. 1= 1
P.L. 2= 0
P.L. 3= 127
P.L. 4= 0
P.L. 5= 0
  
```



```

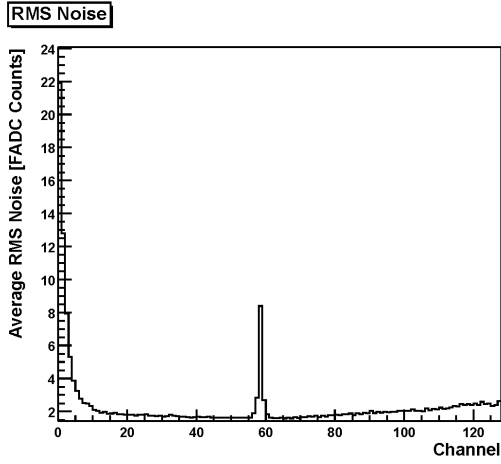
Chip Settings:
DC-Address= 74
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VFS= 60
VSR= 40
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L. 1= 1
P.L. 2= 0
P.L. 3= 127
P.L. 4= 0
P.L. 5= 0
  
```





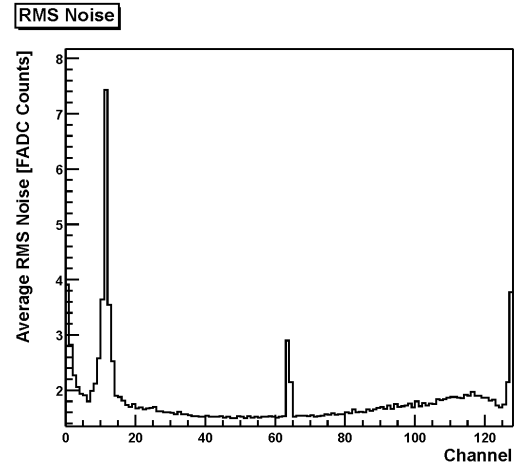
# Module #11 Noise @ 20°C

Chip Settings:  
I2C.Address= 64  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPAR= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSP= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



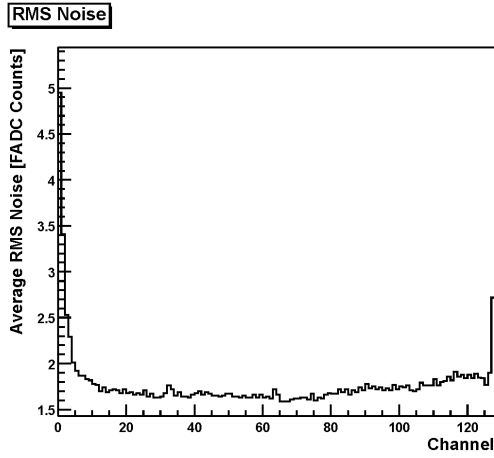
0x40

Chip Settings:  
I2C.Address= 66  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPAR= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSP= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



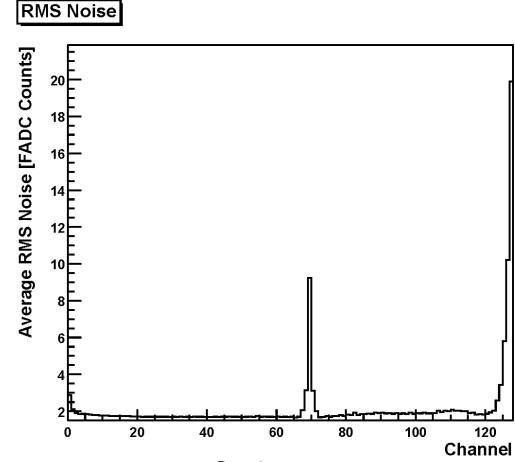
0x42

Chip Settings:  
I2C.Address= 72  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPAR= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSP= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



0x48

Chip Settings:  
I2C.Address= 74  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPAR= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSP= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



0x4a

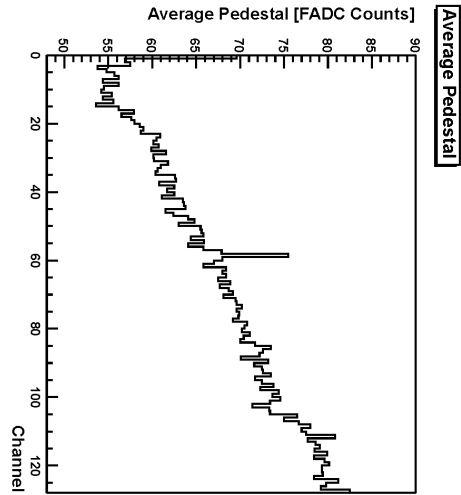


# Module #11 Pedestals @-20°C

```

Chip Settings:
DC-Address= 64
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VRS= 60
VRS= 60
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L1_1= 1
P.L1_2= 0
P.L1_3= 127
P.L1_4= 0
P.L1_5= 0

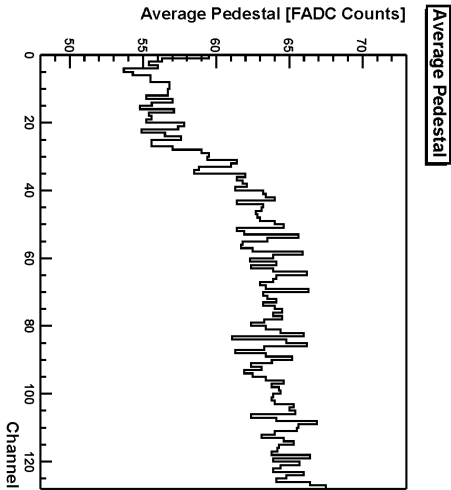
```



```

Chip Settings:
DC-Address= 72
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VRS= 60
VRS= 60
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L1_1= 1
P.L1_2= 0
P.L1_3= 127
P.L1_4= 0
P.L1_5= 0

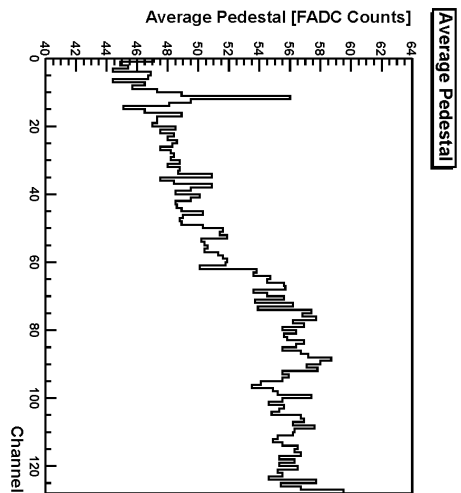
```



```

Chip Settings:
DC-Address= 66
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VRS= 60
VRS= 60
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L1_1= 1
P.L1_2= 0
P.L1_3= 127
P.L1_4= 0
P.L1_5= 0

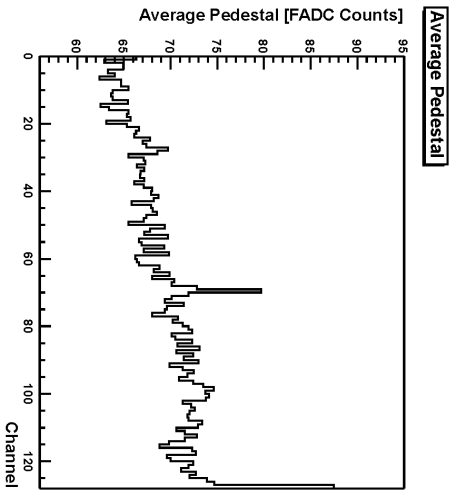
```



```

Chip Settings:
DC-Address= 74
Mode= 11
Latency= 4
IPR= 98
IPCASC= 52
ISR= 34
ISHA= 34
ISR= 34
IPR= 55
MIXIN= 34
ISBAR= 0
ICAL= 29
VFP= 30
VRS= 60
VRS= 60
CMV= 24
CSL= 1
MIXGAN= 4
Error= 0
MIX_Rse= 3
P.L1_1= 1
P.L1_2= 0
P.L1_3= 127
P.L1_4= 0
P.L1_5= 0

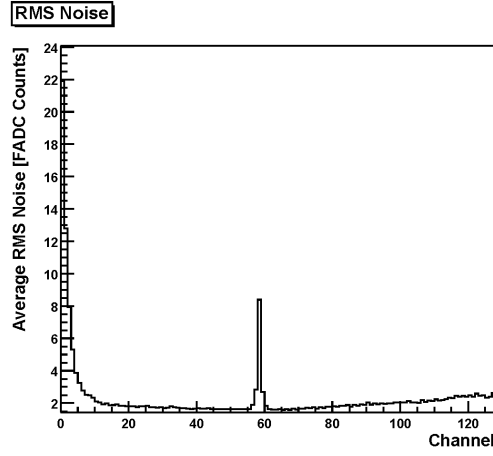
```





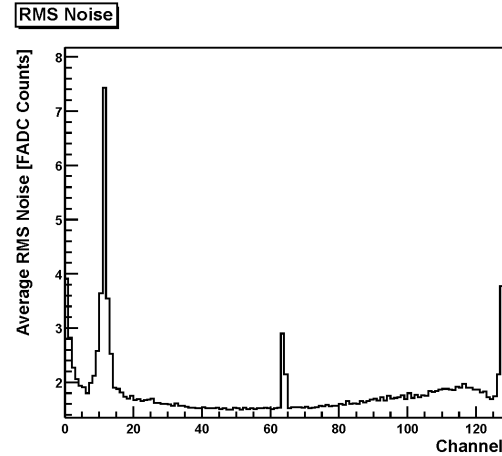
# Module #11 Noise @-20°C

Chip Settings:  
I2C.Address= 64  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPARE= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSF= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



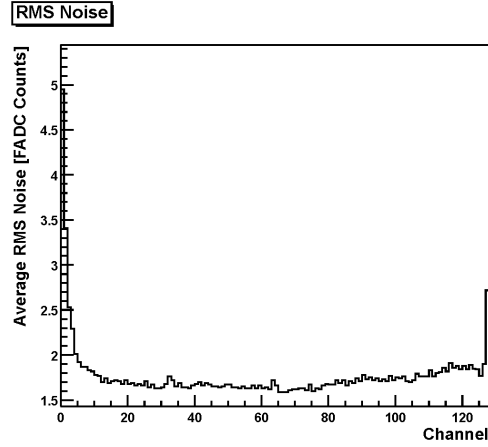
0x40

Chip Settings:  
I2C.Address= 66  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPARE= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSF= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



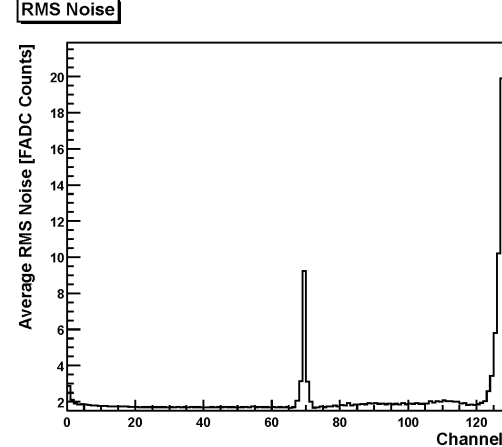
0x42

Chip Settings:  
I2C.Address= 72  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPARE= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSF= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



0x48

Chip Settings:  
I2C.Address= 74  
Mode= 11  
Latency= 4  
IPRE= 98  
IPCASC= 52  
IPSF= 34  
ISHA= 34  
ISSF= 34  
IPSP= 55  
IMUXIN= 34  
ISPARE= 0  
ICAL= 29  
VFP= 30  
VFS= 60  
VPSF= 40  
CDRV= 254  
CSEL= 1  
MUXGAIN= 4  
Error= 0  
MUX\_Res= 3  
PLL\_1= 1  
PLL\_2= 0  
PLL\_3= 127  
PLL\_4= 0  
PLL\_5= 0



0x4a



# *Results*

---

- observations:
  - leakage current  $<1\mu\text{A}$
  - temperature of frame about  $-20^\circ\text{C}$
  - humidity did not exceed 20%
  - no failures of bonds
  - hybrid worked fine

test meets expectations!



## *Further Investigation*

---

- influence of adapter cable on noise
  - signal rising time is little higher
- investigation of noise in test setup
  - where does noise come from
  - Can noise be decreased
  - influence of peltier power supply
- take a closer look at data
- setup new test box!
  - necessary components for operation are there
  - put focus on main issue of test box (testing of hybrids with pitch adapter) but keep old test box to allow other tests



## ***New Test Box***

