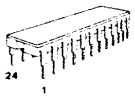
PHYSICAL DIMENSIONS

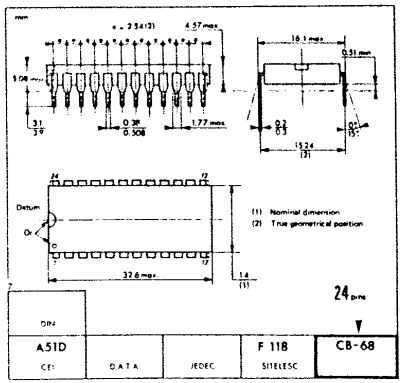
CB-68

J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE



Printed in France

12/12

TS8308

ADVANCE INFORMATION

VIDEO SPEED 8-BIT FLASH A/D CONVERTER

The TS8308 is a monolithic 8-bit HMOS2 parallel (flash) A/D converter designed for high speed conversion.
Parallel sampling is performed via resistor ladder and 256 comparators.
Conversion is accomplished within one pulse.
A very low input capacitance (less than 30 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8308.

Typical characteristics:

- Single +5 V supply.
- ±0.5 LSB differential non linearity.
- 15 MHz sampling rate.
- 5 MHz input signal without sample and hold adjunction.
- Very low input capacitance (max. 30 pF).
- All logic inputs and outputs are TTL compatible.
- Data output: 8-bit binary code + overflow.
- Output buffers for 8-bit data and overflow are 3-state type.
- Accuracy better than 6 mV.
- Pin to pin compatible with RCA CA 3308.

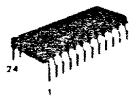
Typical applications:

- TV video digitizing.
- Ultrasound signature analysis.
- Transient signal analysis.
- Radar pulse analysis.
- High energy physics research.
- High speed oscilloscope storage/display.
- General purpose hybrid ADCs.
- Optical character recognition.
- Digital signal processor data acquisition systems.
- Satellite operations.
- Portable video speed products.
- Video printer.
- Fax machine.
- Image processing.
- Medical imaging.
- All high speed A/D conversion applications where low power and low cost are required.

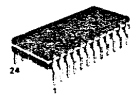
HMOS2

VIDEO SPEED
8-BIT FLASH
A/D CONVERTER

CASE CB-68



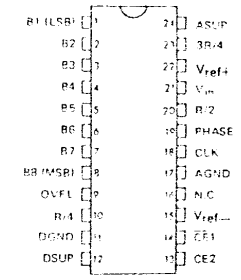
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE

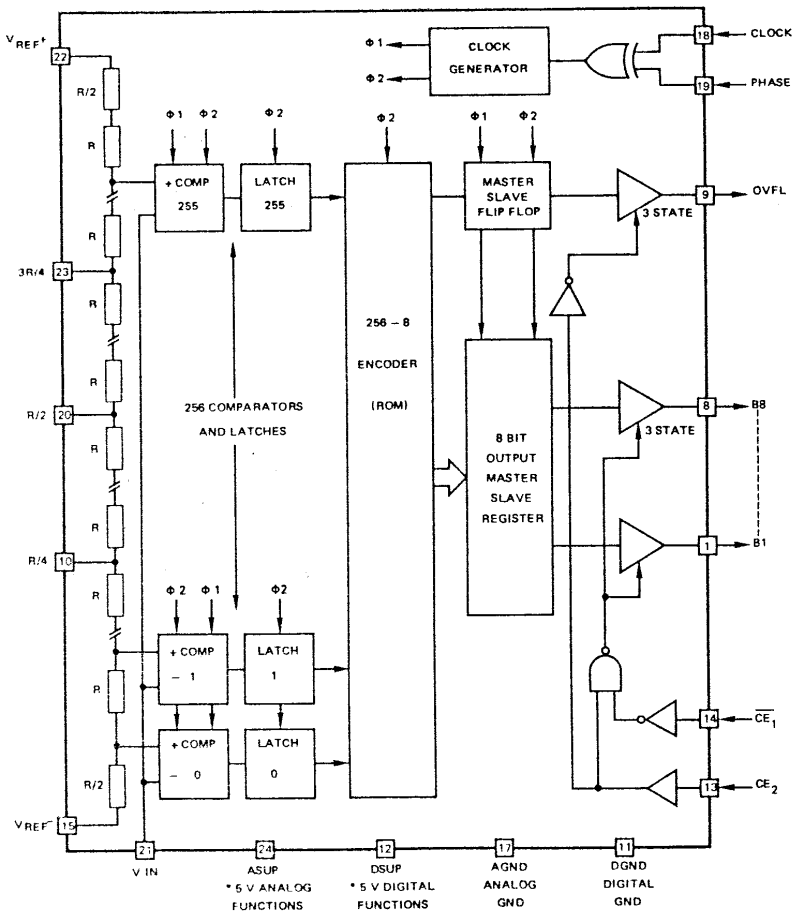
Ceramic package (C Suffix) is also available

PIN ASSIGNMENT



43-45, Avenue de l'Europe - 78140 VÉLIZY-FRANCE - Tél. (1) 39.45.37.19 Télex 240780F

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Number	Function	Description
B_1 (LSB) to B_8 (MSB)	O	1 to 8	Output data	Tristate buffer outputs
OVFL	O	9	Overflow status line	This line is set to logical "1" when the input signal is higher than the $V_{REF}+$ voltage. All data (B_1 to B_8) are set to logical "1"
R/4	I	10	First quarter reference	Access to the first quarter reference voltage
DGND	I	11	Digital ground	
DSUP	I	12	Digital supply	
CE2	I	13	Tristate command	CE2 = "0": tristate for both overflow status and data lines
$\overline{CE1}$	I	14	Tristate command	CE2 = "1": overflow valid out data lines valid only if $\overline{CE1}$ = "0"
$V_{REF}-$	I	15	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
NC		16	Non connected	
AGND	I	17	Analog ground	
CLK	I	18	Clock input	TTL levels
PHASE	I	19	Phase input	When phase is "0" the input signal is sampled on the falling edge of the input clock. When phase is "1" the input signal is sampled on the rising edge of the input clock
R/2	I	20	Half reference	Access to the half reference voltage
V_{IN}	I	21	Analog input	
$V_{REF}+$	I	22	Upper reference	Access to the upper reference voltage. A voltage source must be applied
3 R/4	I	23	Third quarter reference	Access to the third quarter reference voltage
ASUP	I	24	Analog supply	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1) (1)	DSUP ASUP	- 0.3 to + 7 - 0.3 to + 7	V V
Storage temperature	T_{stg}	- 55 to 150	°C
Operating temperature	T_{oper}	0 to 70	°C
Power supply current	IDSUP IASUP IDGND IAGND	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to + 7	V

Note: (1) With respect to AGND = DGND

ELECTRICAL OPERATING CHARACTERISTICS

ASUP = DSUP = 5 V, AGND = DGND = 0 V, V_{ref-} = 0 V, V_{ref+} = 3 V, Phase = 1, F_S = 14.8 MHz, F_C = 4 MHz

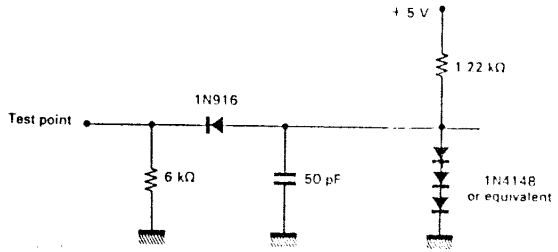
Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N			8	
Linearity error (Peak to Peak)*	ILE			4	LSB
Differential linearity error	DLE		1/2	0.7	LSB
Quantizing error	QE	— 1/2		+ 1/2	LSB
Aperture time	tAP		250		ps
Voltage supply	ASUP, DSUP	4.75	5	5.25	V
Power dissipation (4 MHz):					
Analog supply	PDA		350	450	mW
Digital supply	PDD		90	150	mW
Maximum sample rate	F_S	15		20	MHz
Analog bandwidth	F_C	3.5	5		MHz
Reference ladder					
Lower reference voltage	V_{ref-}	0	0		V
Upper reference voltage	V_{ref+}	1	2	ASUP-1.5	V
Full scale range		1	2	ASUP-1.5	V
Ladder resistance	V_{ref}	400	550	900	ohm
Input capitance	CIN			30	pF
Logic output low voltage	V_{OL}			0.4	V
high voltage	V_{OH}	2.4			V
Digital input low voltage	V_{IL}			0.8	V
high voltage	V_{IH}	2.4			V
Total harmonic distorsion	HD		— 37	— 34	dB
HF gain	GHF			0.4	dB

* See integral non linearity template

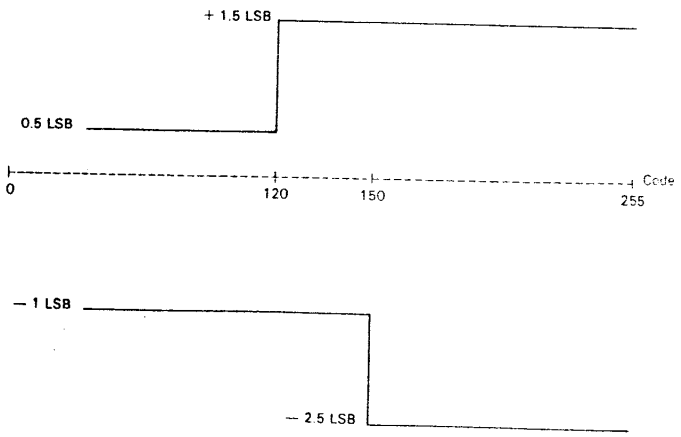
DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Clock pulse width	t_{cl}	25			ns
	t_{ch}	25			ns
Clock rise time	t_{cr}		5		ns
Clock fall time	t_{cf}		5		ns
Outputs progag. (1)	tP		25	40	ns
Outputs transient (1)	tTHL			25	ns
	tTLH			25	ns

(1) Note:



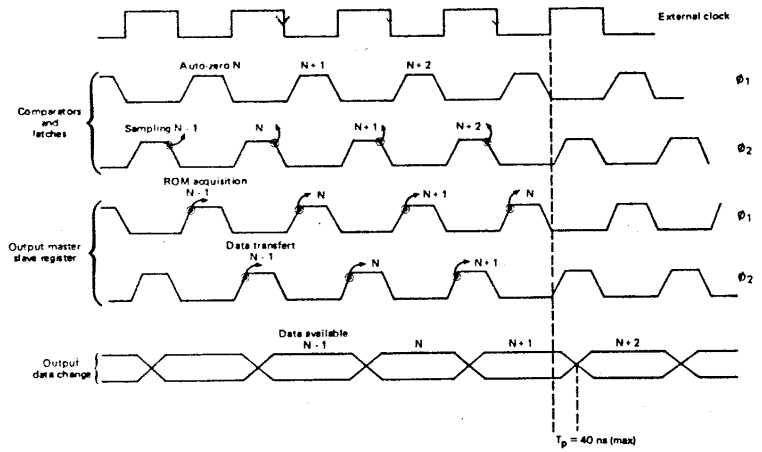
INTEGRAL NON LINEARITY TEMPLATE:



Conditions: 1/4, 1/2 and 3/4 pins free, F_S = 12.5 MHz, F = 3.125 kHz (slope).

Note: Applying a low impedance DC voltage (V_{ref}/ 2) on pin R/2 allows to obtain an integral non linearity better than ± 1 LSB from code 0 to 255.

TIMING DIAGRAM (PHASE = " 0 ")



NB : If phase is set to "1", the external clock is inverted inside the circuit

FUNCTIONAL DESCRIPTION

Circuit TS8308 includes:

- a sequencer generating internal clock,
- a core ensuring conversion,
- an output circuit delivering digital data,
- the sequencer generates 6 internal clocks from pins CLK and PHASE:

Internal phases	Circuits concerned	Function	Value (PHASE = 0)
Φ 1	Comparators	Autozero	$\overline{CLK}$
Φ 2	Comparators	Sampling and comparison	CLK
Φ 3	Latches	Storage	Φ 2 + D
Φ 4	Encoder	Transmission	Φ2 + D
Φ 5	Output master/slave flip - flop	Sampling	Φ 1 + D
Φ 6	Output master/slave flip - flop	Storage	Φ 2 + D

N.B.: D is a time-delay introduced to compensate the signal propagation.

- the core includes:
  - A resistor linear network delivering 256 reference voltages distributed linearly between external reference voltages V_{ref+} and V_{ref-}. Access to quarter (R/4), half (R/2) and three quarter (3R/4) bridges enable the following:
    - either improve linearity by externally forcing reference voltages,
    - filter disturbances going through the bridge by means of external capacitors,
    - or delinearize the bridge by means of external resistors (law of linear compression by blocks).
  - A set of 256 voltage comparators parallel connected across the 256 taps of the reference bridge and the input analog signal which defines the 256 (2^8) quantification levels.
    In first phase Φ1, these comparators store their flip-flop threshold then, in phase Φ2 they compare the thresholds with the input signal.
    The comparators with an input signal voltage lower than the reference voltage present a given state at the output, the others present the complementary state.
    The 256 comparators output is stored in 256 latches at the end of phase Φ3 = Φ2.
  - A 256 to 8 decoder detecting the transition between the comparators in a given state and the ones in the complementary state.
    The line enabled corresponds to the last comparator which has tripped, i.e. the comparator with the reference voltage nearest by default to the input signal.
  - A ROM following the decoder and coding over 8 bits the detected comparison chain in binary.
    If the input signal is lower than the lowest reference voltage (1st comparator), code 0 is written at the output.
    If the input signal is higher than the upper most reference voltage (256th comparator), code 255 is written at the output and overflow bit is set to 1
- The output stage consists of 9 identical parts (8 bits and overflow) each formed of a flip-flop D connected to the ROM output with an output buffer. This buffer is enabled on phase Φ6 = Φ2 and includes a selective high impedance command
  Inputs $\overline{CE1}$ and CE2 switch the output bits to this 3rd state (with overflow bit if required) in order to facilitate the following*:
  - parallel connection of the 2 converters thus providing a double sampling frequency while maintaining an 8 bit resolution,
  - series connection of the 2 converters providing a 9 bit resolution while maintaining a 20 MHz sampling frequency.

$\overline{CE1}$	CE2	B1,...B8 in 3rd state	B9 (OVFL) in 3rd state
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	Yes	No

* See application information.

TYPICAL EVALUATION CIRCUIT *

The general circuit used for the flash converter in typical conditions (8 bits, 20 MHz) is represented on figure 1.

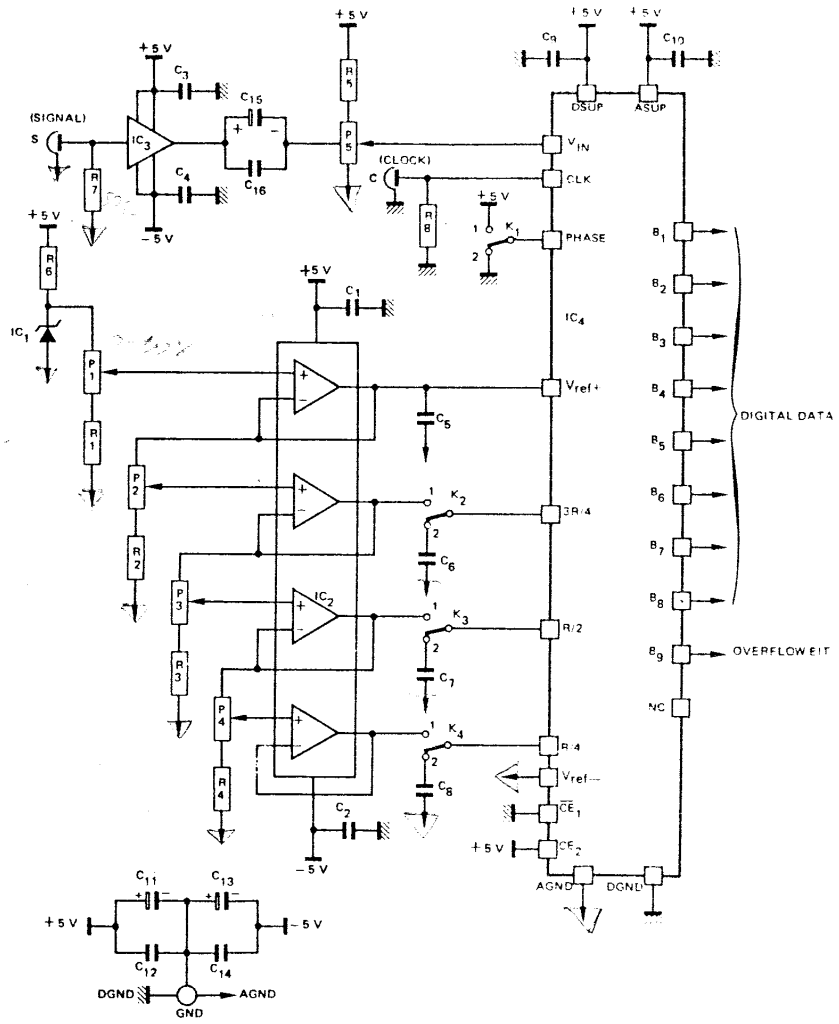
- Voltage reference
  Flash converter requiring a positive reference voltage (V_{ref+}) ranging from 1.5 V to 3 V (typ. 2 V), the circuit generates a reference voltage of 2.5 V from the power supply voltage (+5 V) and a precision regulation diode (IC_1).
- Resistor bridge reference voltages.
  The circuit allows to access some particular points on the resistor bridge. These points correspond to 3/4, 1/2 and 1/4 of the bridge total resistance. This feature enables use of the flash convertor in two ways:
  - in linear operation with these 3 points grounded by uncoupling capacitors in order to filter disturbances along the bridge (K2, K3 and K4 in position 2),
  - in non-linear operation with the following 2 functions:
    - improvement in flash converter integral linearity by forcing the 3 points to their corresponding voltages (K2, K3 and K4 on poisition 1),
    - implementation of a non-linear conversion law (compression law for instance) in order to better observe the results of the conversion on one part only of the transfer characteristic (K2, K3, K4 on position 1).
- Analog signal.
  The input analog signal must be driven by a wide band buffer amplifier (IC_3) with a very low output impedance.

* For typical application circuit, the same surroundings can be used.

In order to eliminate the almost uncontrollable offsets introduced by the source generator or buffer amplifier proper, two capacitors parallel mounted (C_{15} and C_{16}) are added in series after the amplifier. For low frequencies (< 1MHz) tantalum capacitor (C_{15}) is used as a short-circuit; for higher frequencies (> 1 MHz) the ceramic capacitor (C_{16}) is used as a short-circuit.
After these capacitors, a potentiometer (P5) with the middle point connected to the flash converter input adds a DC component to the input signal. The signal thus obtained has an overage value different from zero, lying between V_{ref-} and V_{ref+} and which can be converted by the flash converter.

- Clock signal.
  Clock signals are TTL or CMOS signals. The PHASE command is used to invert (K_1 on position 1) or not (K_1 on position 2) the external signal.
- Considerations on electrical layout.
  A certain number of elementary precautions should be taken in the electrical layout when using high frequencies.
  The main ones are as follows:
  - a ground plane for the components,
  - the ground tracks corresponding to the various signals (clock, input signal, references) are separated and connected together to a single point,
  - a star distributed power supplies (idem for ground) to avoid any possible loop,
  - a maximum capacitive uncoupling as close as possible to each circuit.

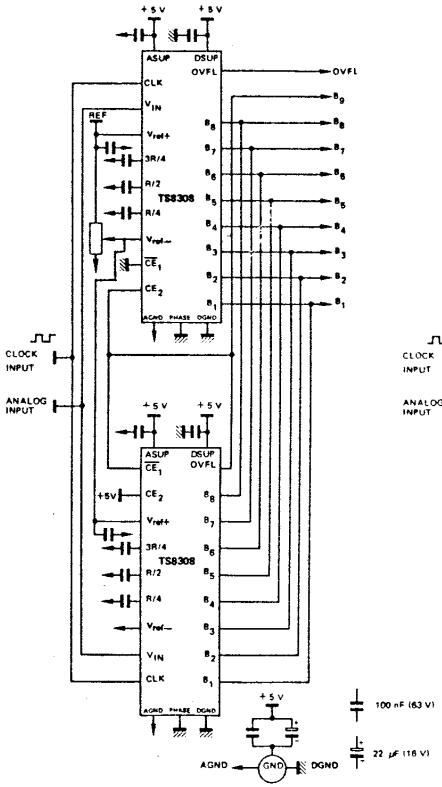
TYPICAL EVALUATION CIRCUIT (continued)



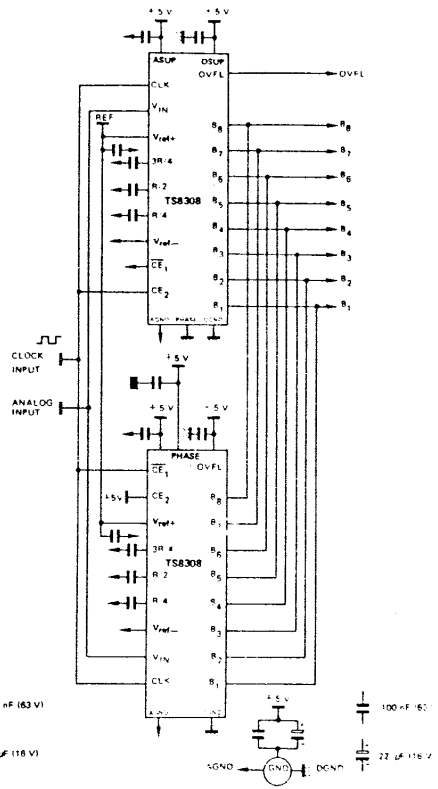
8 BIT RESOLUTION CONFIGURATION 20 MHZ SAMPLING RATE

Component	Value	Component	Value
R1	5.6 KΩ (1/4 W)	C1	100 nF 63 V
R2	3.3 KΩ (1/4 W)	C2	100 nF 63 V
R3	1.2 KΩ (1/4 W)	C3	100 nF 63 V
R4	560 Ω (1/4 W)	C4	100 nF 63 V
R5	10 KΩ (1/4 W)	C5	100 nF 63 V
R6	2 KΩ (1/4 W)	C6	100 nF 63 V
R7	47Ω (1/4 W)	C7	100 nF 63 V
R8	47 Ω (1/4 W)	C8	100 nF 63 V
P1	10 KΩ (multiturns)	C9	100 nF 63 V
P2	10 KΩ (multiturns)	C10	100 nF 63 V
P3	10 KΩ (multiturns)	C11	22 µF 16 V (Tantalum)
P4	10 KΩ (multiturns)	C12	100 nF 63 V
P5	10 KΩ (multiturns)	C13	22 µF 16 V (Tantalum)
IC1	TDB 0136	C14	100 nF 63 V
IC2	TDB 0084	C15	68 µF 16 V (Tantalum)
IC3	LH 0002	C16	100 nF 63 V
IC4	TS 8308		

TYPICAL APPLICATION



TYPICAL TS8308 9 BIT RESOLUTION CONFIGURATION
20 MHz SAMPLING RATE



TYPICAL TS8308 8 BIT RESOLUTION CONFIGURATION
40 MHz SAMPLING RATE